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Lessons Learned from Low-Frequency Noise Studies on Fully Depleted UTBOX Silicon-on-Insulator nMOSFETs

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Introduction. Non-intentionally doped Fully Depleted (FD) Ultra-thin Buried Oxide (UTBOX) SOI offers several advantages from a viewpoint of the suppression of dopant-related variability and short-channel effects [1]. There is also interest in using such devices as 1-transistor (1T) floating-body RAM (1T-FBRAM) cells [2,3]. For the latter applications, charge retention is one of the critical parameters, requiring a tight control of defect-related carrier generation and recombination (GR). One of the techniques which lends itself nicely to this purpose is low-frequency (LF) noise spectroscopy, which can reveal GR centers in the gate dielectric or the silicon film [4,5]. It is the aim of this overview paper to summarize the LF noise behavior of UTBOX FD SOI nMOSFETs developed for 1T-FBRAM applications and to show how the observed flicker and GR noise can be utilized for analyzing defects present in the devices.

2. Experimental conditions. The FD SOI nMOSFETs studied have been fabricated on SOI substrates with nominally 10 nm BOX and 20 or 10 nm Si film thickness (t_{Si}). Transmission Electron Microscopy reveals that the actual values for the short-channel devices studied are closer to 18 nm (BOX) and 14 and 6 nm for t_{Si}. Different types of gate stack have been investigated with 5 nm thermal SiO_2 (t_{ox}) as the reference, but also HfO_2-based high-k devices have been analyzed. Processing splits with or without extensions have been compared, whereby extensionless structures may offer a higher retention time [3]. The device width W=1 μm and different effective lengths (105 nm or 69 nm) were studied. Noise measurements have been mainly performed in linear operation (V_{DS}=0.05 V) and with the back-gate grounded.

3. Flicker noise and coupling. The observed 1/f-like noise is dominated by number fluctuations, i.e., it originates from trapping in the gate oxide, both for the front-gate and back-gate noise power spectral density (PSD). In fact, the use of UTBOX structures enables to experimentally study the coupling between the back and front interface on the PSD. Figure 1 shows that both are linearly correlated, whereby the slope can be explained by considering the noise coupling factor [6,7]. Due to this, the effective front-gate oxide trap density (N_{ot}) is higher than at the back-gate and should be corrected for it.

4. GR noise and noise variability. In some devices, excess GR noise, giving rise to a Lorentzian spectrum can be found. It has been shown that this GR noise can explain the variability in the noise PSD of the UTBOX transistors [7,8].

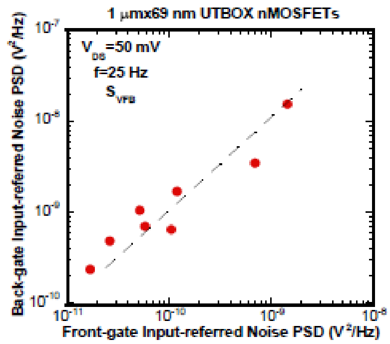

Fig. 1. Back- versus front-channel average input-referred noise PSD at flatband (V_{GS}~V_T), f=25 Hz and V_{DS}=50 mV for a set of 1 μm×69 nm UTBOX nMOSFETs with t_{Si}≈14 nm and t_{SiO2}=5 nm.

In order to explain the orders of magnitude difference in Lorentzian amplitude that can be found, a dedicated model has been developed [9], which at the same time explains the gate voltage dependence of the main parameters (plateau amplitude and time constant).

4. Random Telegraph Noise. From the extracted trap concentrations, it is clear that the GR noise is generated by only a handful of traps – similar as the retention time, with similar activation energy. It is well-known that if only a few traps are present in the gate oxide, the 1/f noise transforms into so-called Random Telegraph Noise (RTN), also giving rise to a Lorentzian spectrum. The question arises how to distinguish RTN from GR noise in the silicon film. It will be proposed that studying the noise in both the front and back-channel may enable to distinguish the different cases [10]: when a similar Lorentzian is present in both cases, one can assume that the traps are present in the silicon film. If on the contrary, the Lorentzian is only found in the front or back-gate spectrum with the other channel accumulated, than one can conclude that the trap resides in the front or back-gate oxide.

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