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Visualization of Plasma Etching Damage of Si Using Room Temperature Spectroscopic Photoluminescence

Shiu-Ko Jang Jian[1], Chih-Cherng Jeng[1], Ting-Chun Wang[1], Chih-Mu Huang[1], Ying-Lang Wang[1], and Woo Sik Yoo[2]

[1]Taiwan Semiconductor Manufacturing Company, Ltd., No. 1-1, Nan-Ke Rd., Science-Based Industrial Park, Tainan, 741-44, Taiwan
[2]WaferMasters, Inc., San Jose, CA 95112, USA

Plasma processes have been widely used in the manufacturing of semiconductor devices. Etching of polysilicon, dielectric and metal films, dielectric deposition, cleaning, sputtering, photoresist stripping and ion implantation commonly use plasma assisted processes. Devices fabricated on Si wafers are directly exposed in the plasma (charged particles such as ions and electrons) ambient.

Plasma induced degradation of gate oxides in metal-oxide-semiconductor (MOS) devices due to electrical charging has been observed. Plasma induced damage (PIDs) is a growing concern for plasma processing of advanced devices with very small feature sizes. [1-5]

Characterization of PIDs often requires special types of test wafers with various antenna structures and/or electrical test of devices after completion of fabrication. Development of easy-to-use PID visualization techniques, without special test structures, would be extremely useful for in-line process monitoring and PID minimization applications.

In this paper, room temperature photoluminescence (RTPL) spectroscopy was proposed as a PID visualization technique. As an application example, 200 ~ 700 nm thick oxide films on 300mm wafers (SiO_2/Si) grown by plasma enhanced chemical deposition (PECVD) were plasma etched under different rf power conditions. Oxide etch rate, oxide uniformity and RTPL spectra/intensity were measured and characterized.

RTPL spectra were measured using WaferMasters' MPL-300 system under three excitation wavelengths (532, 650 and 827nm) which have different probing depths. Exposure time was varied from 100 to 1000 ms per measurement site. For detailed wafer mapping, 15,660 points per wafer per excitation wavelength were measured. A very strong rf power dependency of oxide etch rate and RTPL spectra/intensity was observed and quantified. Significant localized weakening of RTPL intensity was observed from SiO_2/Si after plasma etching under un-optimized conditions. A distinct pattern of PID's was observed representative of showerhead patterns, common to a typical plasma etching system. The RTPL technique did not use any special test structures on the wafer.

Factors affecting RTPL intensity under different excitation wavelengths will be discussed in connection with observed PID distribution and generation mechanisms. Device performance wafer maps will be compared with multiwavelength RTPL maps and their correlation will be discussed from inline process monitoring and PID visualization points of view.

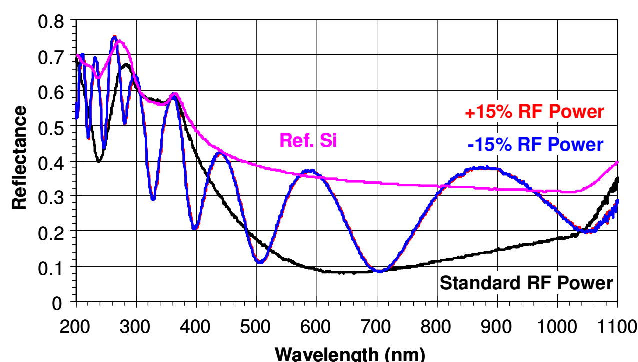

Figure 1. UV-VIS-NIR reflectance spectra of SiO_2/Si wafers after plasma etching under three rf power conditions. Reflectance spectra of base Si wafer is plotted as reference.

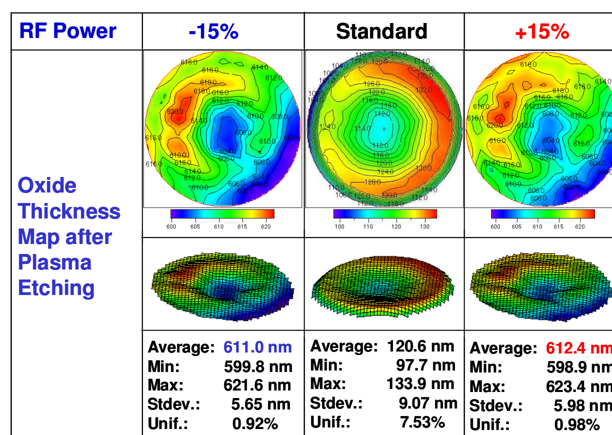

Figure 2. 2D and 3D oxide thickness contour maps after plasma etching under three different rf power conditions.

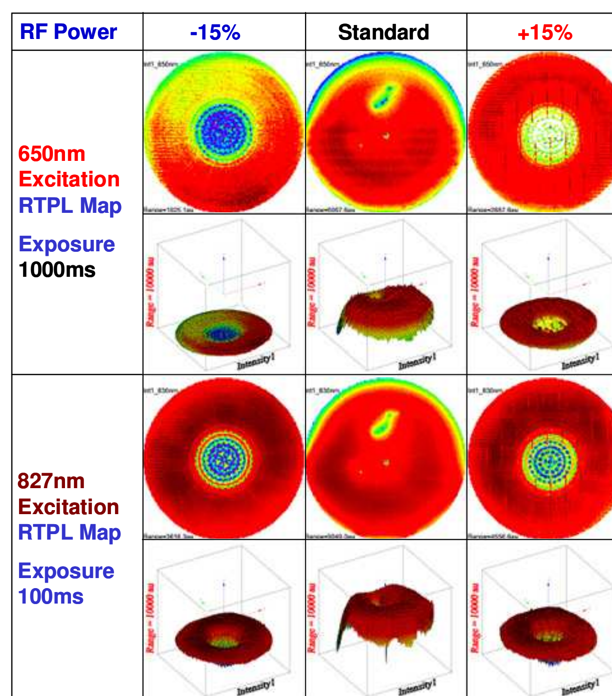

Figure 3. multiwavelength RTPL intensity maps of SiO_2/Si after various rf power plasma etching conditions.

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