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A study of polysilicon gate etch uniformity in 300 mm silicon wafers

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Experimental data show that the gate length tends to be smaller in the middle of the silicon wafer and also at the silicon wafer edge. In-line CD (critical dimension) data will be presented to support the above claim. This is also supported by device measurements. Physical mechanism responsible for the experimental observation will be provided.

The on current and off current of MOS transistors are sensitive to variations of the effective channel length. The effective channel length depends on the polysilicon gate length after polysilicon gate etch.

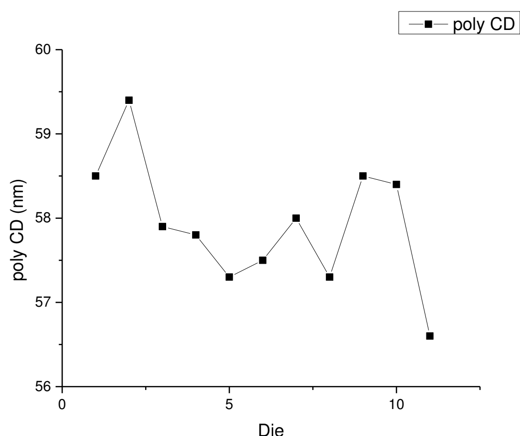

Fig. 1 FICD (critical dimension after etch) distribution for polysilicon gate length vs. Die. It can be roughly seen that the smallest poly CD occurs in the middle of the wafer or at the 2 wafer edges.

It can be roughly seen in Table I that the gate length after polysilicon gate etch is smallest in the middle of the silicon wafer and also at the silicon wafer edge.

Experimental measurement of the on current and off current of MOS transistors show up a similar trend like in-line CD measurement. The on current and off current of devices tend to be largest in the middle of the silicon wafer and also at the silicon wafer edge. Similarly, DIBL (drain induced barrier lowering, which can be used as a measure of the effective channel length) tend to be largest in the middle of the silicon wafer and also at the silicon wafer edge.

The physical mechanism responsible for stronger etch in the middle of the silicon wafer is just a "symmetry" effect. Etch machines based on Inductively Coupled Plasma (ICP) tend to etch more strongly in the middle of the etch chamber [1]-[2]. The physical mechanism responsible for stronger etch at the silicon wafer edge is due to weaker "etch loading" at the silicon wafer edge [3]-[4]. The combined effect of the above two mechanisms is that the polysilicon gate length shows up some sort of "inverted W" distribution. In addition, the FICD distribution shows up some sort of instability from wafer to wafer even though it roughly obeys an "inverted W" distribution. It is believed that the above mentioned instability is related to the instability reported by Soberon et al. [5].

In conclusion, experimental data show that the gate length tends to be smaller in the middle of the silicon wafer and also at the silicon wafer edge. Both in-line CD data and device measurement data support this conclusion. However, it also appears that the gate length distribution has some sort of instability from wafer to wafer.

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