Tunnel FETs for Mixed-Signal System-on-Chip Applications

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Owing to its different current injection mechanism, a tunnel field-effect transistor (TFET) can achieve a sub-60mV/decade subthreshold swing at room temperature [1], which makes it very attractive in replacing a metal-oxide-semiconductor FET (MOSFET) for low-power logic applications. In the past couple of decades or so, the analog performance of the scaled CMOS devices has also received considerable attention, particularly for mixed-signal system-on-chip (SoC) applications, where the analog circuits are realized together with the digital circuits and memories in the same integrated circuit in order to reduce the cost and improve the performance. A good output current saturation is necessary for a device in order to qualify itself for analog applications. Such a good output current saturation is normally observed for a long-channel MOSFET due to pinch-off near the drain end of the channel at larger drain voltages. Short-channel effects, such as drain-induced barrier lowering (DIBL), deteriorate the analog performance of a scaled MOSFET.

It is well-known that, although some device structures for a TFET show a good drain current saturation in their output characteristics, the others do not. The construction of the channel plays an important role in determining whether or not a TFET can have a good output current saturation [2]. The main criterion for this is that the thickness of the silicon body for a single-gate SOI or for a double-gate TFET or the fin width for a Fin-TFET should be small enough, so that the applied gate voltage can influence the potential and, hence, cause accumulation/depletion/inversion in the entire channel region. When such a device is turned on by applying a suitable gate voltage, the entire channel becomes populated with carriers supplied by the drain at low drain voltages. At larger drain voltages, the carriers are pulled back from the entire channel region to the drain resulting in pinch-off of the entire channel. As a result, the channel resistance becomes so high that the lateral electric field from the drain can no longer penetrate the channel and, hence, the tunneling junction remains unaffected for further increase in drain voltage that in turn results in a perfect output current saturation.

As the thickness of the channel is increased, the gate loses control of the part of the channel that is away from the insulator-semiconductor interface. This part of the body remains charge neutral even at larger drain voltages, which acts like a resistor of moderate value. As a result, although the surface region of the channel gets more and more depleted of carriers for increasing drain voltages resulting in a large resistance there, the lateral electric field, through the charge neutral part of the body, can still penetrate and, hence, influence the tunneling junction. This in turn results in increasing output current with drain voltages, similar to DIBL, which deteriorates the analog performance of the device [3].

A comparison of the analog performance parameters between a double-gate TFET of 50 nm gate length with a 10-nm-thick silicon body and a similarly-sized MOSFET reveals [3] that, although the transcunductance g_m is lower in a TFET than that in a MOSFET by more than an order of magnitude, which is due to low drive current in the TFET, transcunductance-to-drain current ratio g_m/I_D is higher in the TFET, except for small values of the gate over-drive voltage V_{GT}. The g_m/I_D is an important device performance parameter for analog circuits, since the transconductance represents the amplification delivered by the device, and drain current represents the power dissipation to obtain the amplification. It may, therefore, be concluded that a TFET is capable of producing higher gain than a MOSFET at the same power level. Because of good output current saturation for the TFET due to the reason mentioned earlier, the output resistance R_O is found to be extremely high for such device, which is more than 2 orders of magnitude higher than that for the MOSFET. A comparison of intrinsic gain $g_m.R_O$ between the TFET and the MOSFET reveals that the gain is in the order of 10^3 for the TFET as compared with 10^2 for the MOSFET. Although g_m is less, extremely high value of R_O results in such high value of the intrinsic gain for the TFET. Unity-gain cut-off frequency f_T is, however, found to be lower in the TFET than that in the MOSFET, by more than an order of magnitude. The reduced f_T in the TFET is mainly due to the reduced g_m, and partially due to the higher value of the total capacitance (C_{gs} + C_{gd}) in such devices.

Significantly higher voltage gain, by more than an order of magnitude, is also demonstrated for a current source complementary TFET amplifier as compared with its CMOS counterpart [3].

It is, therefore, concluded that a TFET with a thin body or a Fin-TFET of relatively small fin width can be very attractive for mixed-signal SoC applications particularly at moderate frequencies.

References

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