

Impact of Dynamic Body Floating Effect on Low-Energy Operation of XCT-SOI CMOS Devices with Aim of sub-20-nm Regime

Y. Omura, D. Ino, and D. Sato
 Grad. School Sci. and Eng., Kansai University,
 Suita, Osaka 564-8680, Japan

This paper considers the dynamic and standby power dissipation characteristics of the scaled XCT-SOI MOSFET[1,2]. Here, first, we analyze the low-energy operation of XCT-SOI CMOS circuits; the model proposed here strongly suggests that the ‘dynamic body-floating effect (DBFE)’ substantially reduces the operation power consumption. Great advantages of the design methodology are also elucidated. In addition, this study addresses the reality of sub-20-nm-long gate XCT devices and a scaling scheme to suppress the standby power consumption for future low-energy applications.

The schematic device structure is shown in Fig. 1. In an n-channel SOI XCT device, the n-channel SOI MOSFET and p-channel JFET are self-merged and the electron current of nMOSFET is relayed to the hole current of pJFET in series. The XCT device offers negative differential conductance (NDC) in the saturation region of drain current [1,2]. The NDC successfully suppresses the SCE by the effective substrate bias effect. Since the XCT device has active body contact, from pJFET, the conventional ‘static body-floating effect (SBFE)’ is eliminated automatically.

Here we advance the discussion to better understand XCT-CMOS EXOR circuit features. We concentrate the discussion on the energy ratio of CMOS-EXOR circuits, where energy ratio (ER) is defined as the energy dissipated by the XCT-CMOS EXOR over that of the comparable conventional SOI-CMOS EXOR. Calculation results based on HSPICE simulation results are shown in Fig. 2.

It is seen that the ER value of 1- μm -long gate devices is almost unity regardless of the V_{DD} value assumed. This behavior is reasonable for the following reasons. The energy dissipation of conventional devices, evaluated by the $P_d \cdot t_d$ product, is not a function of V_{DD} due to the simple recognition of the MOS gate capacitor’s charging and discharging operations. It is anticipated that the XCT-CMOS with 1- μm -long gate follows this principle. In the case of 0.1- μm -long gate devices, on the other hand, it is seen that the ER value rapidly falls as V_{DD} rises. Since this is a very interesting result and somewhat mysterious, we discuss below a possible mechanism based on physics. Energy ratio (ER) is defined by

$$ER(\omega) = \frac{C_{Gn,XCT} + C_{Gp,XCT} + C_{Dn,BOX} + C_{Dp,BOX}}{C_{Gn,MOS} + C_{Gp,MOS} + C_{Dn,BOX} + C_{Dp,BOX}}, \quad (1)$$

where $C_{Gn,XCT}$ and $C_{Gp,XCT}$ denote the effective gate capacitance of n -SOI XCT MOS and p -SOI XCT MOS, respectively. We proposed the equivalent circuit model for the XCT-SOI MOSFET (see Fig. 1(c)) and examined the availability of the DFBE model using Eq. (1). The model successfully reproduced the behavior of the energy ratio (ER) (not shown here). In addition, low energy operation of XCT-SOI CMOS circuits was also demonstrated (not shown here).

References

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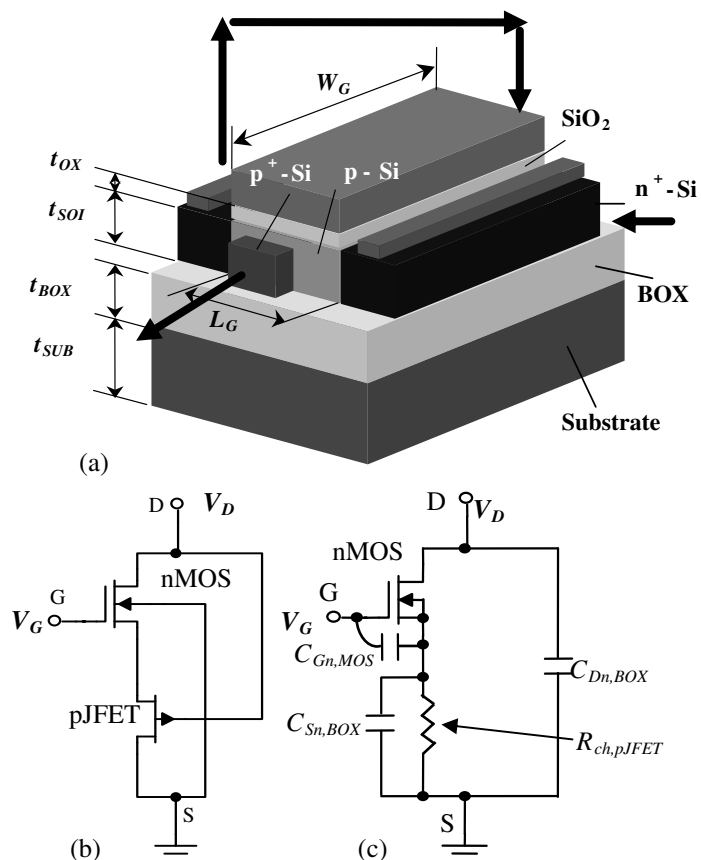


Fig. 1. XCT SOI MOSFET (bird’s eye view and equivalent circuit models). (a) Bird’s eye view of XCT device with parameter definitions and current flow. Arrows reveal the current flow. (b) Basic equivalent circuit model of n-XCT-SOI MOSFET. (c) AC circuit model of n-XCT-SOI MOSFET.

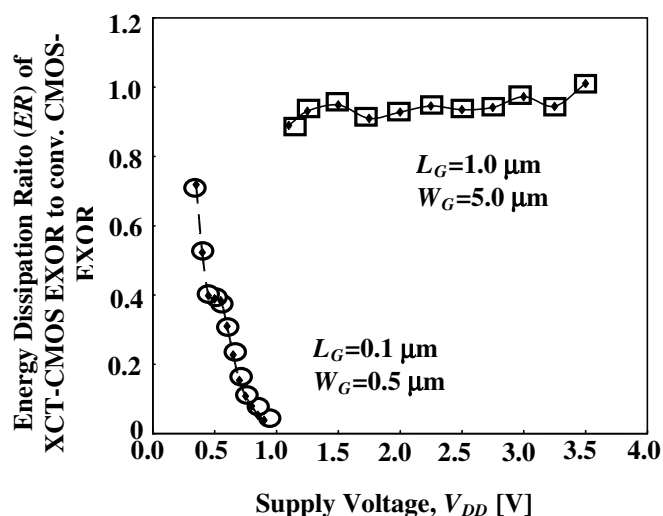


Fig. 2. Simulation results of energy ratio (ER) of the energy dissipation of 1.0- μm -long gate CMOS EXOR and 0.1- μm -long gate CMOS EXOR. The energy ratio is defined by the energy dissipated by the XCT-EXOR divided by that of the conventional CMOS EXOR.