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Investigation of Embedded SiGe Source/Drain for 28nm HKMG PFET Performance Enhancement

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Abstract: Embedded SiGe (eSiGe) is one of the mobility boosters for PFET devices in high performance technologies. In this paper, improved performance through higher drive current is demonstrated by the optimization of the eSiGe in a state-of-the-art 28nm logic flow. In particular, the shape of the deposited eSiGe plays an important role for modulating the compressive stress in the PFET channel. Electrical measurements supported by TCAD process and device simulations, confirm that the optimized eSiGe enables a distinctive strain enhancement at the channel region.

Introduction: For advanced technology nodes, in parallel with ultra shallow junction (USJ) depth scaling and reduced threshold voltage (Vth) variation, high-performance MOSFETs with high-k/metal-gate (HKMG) stacks incorporating stress-inducing SiN liners and eSiGe source/drain have been reported [1-2]. To further improve the device performance, boosting the mobility by incorporating Ge in the channel is one of the possible options. In this work, we present a novel approach which focuses on the eSiGe deposition shape control effect on the strain in the channel region of pFET for 28 nm technology node. The detailed device characteristics are discussed along with integrated Technology – CAD (TCAD) modelling [3-4].

Device Preparation: Fig. 1a shows device fabrication flow. Experiments were carried out on a state of the art 28nm-node platform with HKMG stack in a gate first approach [5-6]. PFET incorporates a channel SiGe for further Vth adjustment and eSiGe as stressor in the S/D [7]. After S/D implant, high thermal budget (>1000°C) for dopants diffusion and activation was utilized.

eSiGe Shape Optimization: In this work we address the effect of eSiGe shape optimization on the strain induced in the cSiGe and subsequently the device performance. The deposition conditions were tuned such that through the adjustment of the growth rate ratio between different crystallographic plane orientations, a (111) facet was formed adjacent to the channel.

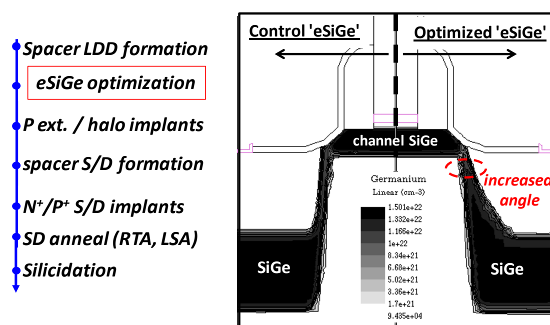

Figure 1: (a) 28nm pFET process flow with SD stress formation and the corresponding simulated TCAD structures (b) showing the control eSiGe (standard, left) and the optimized eSiGe (right) with highlighted channel SiGe (cSiGe) and embedded SiGe (eSiGe).

Modelling: A TCAD suite including process and device simulation capabilities was used. A 2D device structure (Fig. 1b) was first built based on TEM, which then allows to realistically simulate the fabrication process flow including dopant implantation and annealing conditions. The activation, segregation and Transient Enhanced Diffusion (TED) models were successfully applied to simulate diffusion and activation of boron during the annealing steps. A good agreement between simulated and SIMS dopants profiles were achieved. Afterward, TCAD device models and parameters are calibrated based on various electrical data, which account for process induced stresses such as SiGe pockets (PMOS device only) or dual stress liners (DSL).

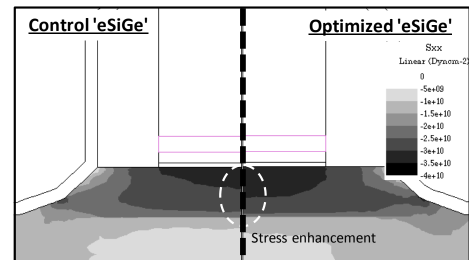

Figure 2: Comparison of longitudinal strain (Sxx) along the channel (x) between control (left) and optimized eSiGe (right).

Optimized eSiGe – Results and Discussion: In this work, TCAD was extensively used to optimize the effect of eSiGe shape on the induced strain in the cSiGe and subsequently on the device performance. Fig. 2 reports the simulated longitudinal stress (Sxx) cartography in the channel region for the control and optimized eSiGe structures as shown on Fig. 1b. Higher stress levels in the channel are achieved for the optimized structure. This leads to a significant performance improvement (+5%) for the optimized eSiGe (Fig.3a: open square vs. filled circle symbols) as confirmed by measurements. The increase of the hole mobility due to stress enhancement is the main driver for such a performance boost (curve not shown here), thus demonstrating that the fine-tuned deposition process allows for a better mechanical stress coupling from S/D to channel in the case of optimized eSiGe. Moreover, the higher Ion/Ioff achieved with the latter structure is obtained without drain induced barrier lowering (DIBL) degradation. A comparison of the Vth roll-off and DIBL of the core pFET device having control (unoptimized) eSiGe or optimized eSiGe are plotted in Fig. 3b. Both splits exhibit the same Vth trend and similar short channel effect (SCE). These results are attributed to the same dopants diffusion and activation. Both trends can be modeled by TCAD. Indeed, the simulated 2D junction shapes reveal that both the control and the optimized eSiGe structures have similar junctions with the same Vth while maintaining a comparable overlap capacitance.

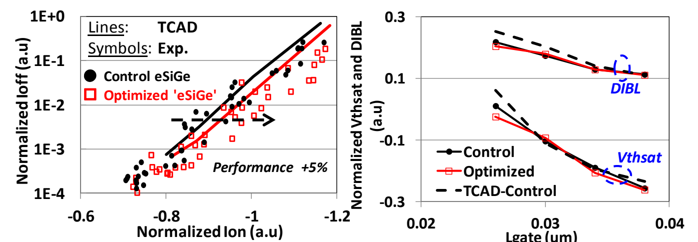

Figure 3: (a) Comparisons of Ion/Ioff performance curve between control and optimized eSiGe for PFET devices. Ion/Ioff improvement is demonstrated with the optimized eSiGe. (b) Comparisons of Vthsat roll-off and DIBL for control vs. optimized eSiGe structures: same Vth and DIBL behavior is achieved. TCAD simulations well reproduce the measured roll-off and DIBL.

Conclusion: Performance improvement of 28nm HKMG PFET device was investigated. The optimization of embedded SiGe, to achieve higher strain coupling between SD and channel region, leads to significant performance improvement without degrading the short channel effects.

References

[1] H.Yin et al., Symp. VLSI Tech., pp. 222, 2007
[2] B.(F).Yang et al., Symp. VLSI Tech., P.126, 2007
[3] Synopsys, “Taurus TSUPREM4 User Guide.” 2010
[4] Synopsys, “Taurus Medici User Guide.” 2010
[5] K. Henson et al., IEDM, pp. 645-648, Dec. 2008
[6] X. Chen et al., Symp. VLSI Tech., pp. 88-89, 2008
[7] T. Ghani et al., IEDM, pp.978–980, Dec. 2003