Capacitance-Voltage Characteristics of Gate-All-Around $In_xGa_{1-x}As$ Nanowire Transistor

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In recent years, III-V MOSFETs has drawn much attention for its high carrier mobility and suppressed short channel effects (SCE). Out of various single/multiple gate structures for CMOS transistors, gate-all-around (GAA) structure has exhibited better immunity to SCE [1]-[3]. Lately, gate-all-around $In_xGa_{1-x}As$ MOSFET with 50nm channel length has been demonstrated with various experimental results [4]. However, Capacitance–Voltage (C-V) characteristic of the device, which is one of the important electrical characteristics of interest for MOS structures, remains to be explored. Here, we present complete C-V characteristics of the GAA $In_xGa_{1-x}As$ nanowire transistor that is yet to appear in the literature. In this work, Finite Element Method (FEM) is used to solve Poisson's equation and Schrödinger's equation self-consistently, considering wave function penetration and other quantum effects to calculate gate capacitance and charge profile for different gate bias voltage.

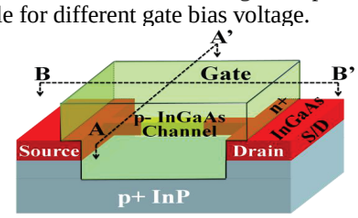

Fig.1. Schematic view of an inversion-mode GAA n-channel $In_{0.53}Ga_{0.47}As$ nanowire transistor with ALD AI_2O_3/WN gate stacks

Now, for C-V characteristics, gate capacitance per unit length is obtained from the following basic concept,

$$C_G = \frac{dQ_{InGaAs}}{dV_G} \quad (1)$$

Where, Q_{InGaAs} is the charge deposited inside $In_xGa_{1-x}As$ channel which is obtained from,

$$Q_{InGaAs} = \int_x \int_y \rho(x,y)\,dy\,dx \quad (2)$$

Fig. 2 shows probability density for 1st Eigen state and conduction band profile under inversion condition as obtained from numerical simulation. Variation of 1st Eigen state (Fig. 3) with gate voltage demonstrates that inversion becomes prominent when discrete Eigen states go down the Fermi level. The saturation capacitance value of typical C-V curves is equal to the gate oxide capacitance. Before any rigorous numerical simulation, this observation can be used to calculate inversion capacitance by approximating the nanowire as cylindrical co-axial cable. The capacitance of the dielectric for such structure is given by,

$$C_{ox} = 2\pi\,\varepsilon_0\varepsilon_r \ln((2t_{ox}+d_{NW})/d_{NW}) \quad (3)$$

For rectangular GAA device, empirically, $\pi d_{NW} = 4W$. Here, t_{ox} and d_{NW} are thickness of the oxide and diameter (film thickness) of the nanowire, respectively and W is the fin-width. Calculated value (1.2×10^{-9}) of capacitance using Eq. (3) is in reasonable agreement with the numerical simulation. Saturation capacitance under accumulation can be obtained multiplying by a factor of $(m_h/m_e)^{0.25}$.

Finally, numerical C-V curves thus obtained are presented in Fig. 4 and have been compared with the result of ATLAS. It reveals a good agreement between quantum mechanical C-V curve and ATLAS simulation with an obvious disagreement with semi-classical C-V. It reiterates the necessity of considering quantum mechanical effects in nano-scale structures. Apparent disagreement between ATLAS and this work around low gate voltage region can be attributed to dis-inclusion of the effects of oxide traps and interface states [5] in the simulation of this work. The outcome of this work will be useful in future CMOS applications and advanced-ULSI designs using gate-all-around nano-scale devices.

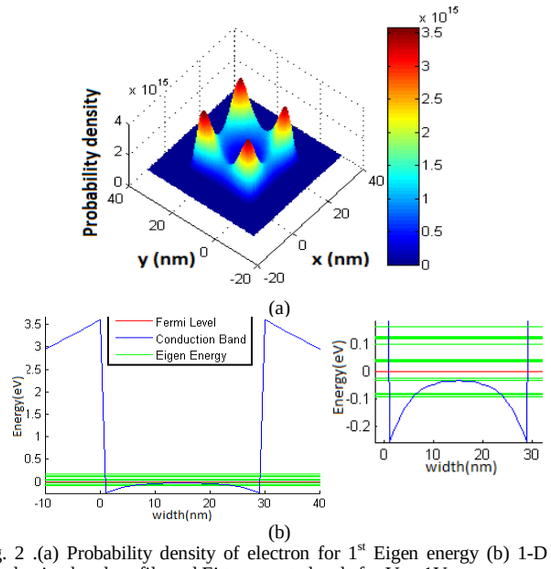

Fig. 2 .(a) Probability density of electron for 1st Eigen energy (b) 1-D Conduction band profile and Eigen energy levels for V_G =1V

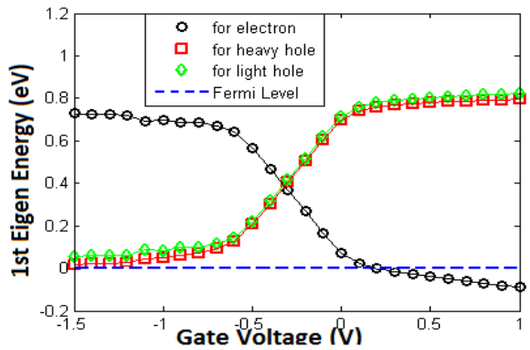

Fig.3. Variation of 1st Eigen energy of electron, heavy-hole and light-hole with gate voltage. It shows that inversion starts when 1st Eigen state of electron crosses Fermi level.

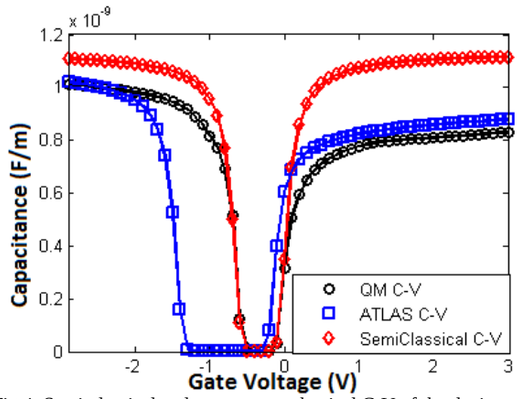

Fig.4. Semi-classical and quantum mechanical C-V of the device used in this study. ATLAS simulation is included for comparison. As, $m_e^* < m_h^*$, saturation capacitance is less in inversion region.

References

[1] Y. Tian et al., *IEDM Tech. Dig.* 895 (2007)
[2] N. Singh et al., *IEEE Trans. Electron Device*, **55,** 3107 (2008)
[3] S. D. Suk et al., *IEDM Tech. Dig.* 552 (2005)
[4] J.J. Gu et al., *IEDM Tech. Dig.* 769-772 (2011)
[5] V. Fomenko et al., J. Appl. Phys., 97, 083711 (2005)