Deep Depletion and Interface Trap Redistribution Behavior in Non-planar MOS with Ultra-thin Oxide Grown by Anodic Oxidation

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In this paper, the non-planar MOS device with ultra thin oxide grown by anodic oxidation was manufactured as shown in Fig. 1. The oxide thicknesses of non-planar sample are non-uniform on different crystal curvatures. A concave corner induced larger electric field crowding in anodic oxidation, therefore, a concave profile has thicker oxide thickness than convex profile. Moreover, we find the deep depletion (D.D) electrical characteristics between the non-planar and planar samples are different as shown in Fig. 2. In the planar sample, the C-V curve of D.D has two regions, i.e., depletion-inversion region (region 1), and bulk deep depletion (region 2). Moreover, the non-planar sample has different two regions, i.e., minority carrier crowding induced low frequency effect (region A) and corner E-field crowding induced D.D (region B). In Fig. 3., the deep depletion behavior of non-planar sample after constant voltage stress (CVS) was explored. Under the fresh condition, the low frequency effect was caused by minority carrier crowding due to the thick oxide in concave corner. After the stress of -2V for 1000s, the low frequency effect was degraded due to the leak of minority carrier at the corner. Following, the corner E-field crowding induced D.D. was enhanced under the stress conditions of -3V and -4V for 1000s. Two peaks phenomenon in interface trap capacitance (C_{it}) versus V_G-V_{FB} curve after CVS was observed as shown in Fig. 4. However, the planar one exhibits only single peak. The two peaks phenomenon of non-planar sample can be explained by non-(100) crystal orientations at the sidewall and non-uniform portion after RIE etching. The cross point between the two distributions in C_{it} is at $V_G - V_{FB}$=0.3(V), which corresponds to the energy level of surface trap (E_t) just equal to intrinsic Fermi energy level (E_i). The non-(100) crystal effect induces another interface trap of acceptor-like in non-planar sample which corresponds to the energy level of Et > Ei. On the contrary, the interface trap of planar sample is mainly donor-like. Nevertheless, the study of non-planar structure is of importance.

ACKNOWLEDGMENTS

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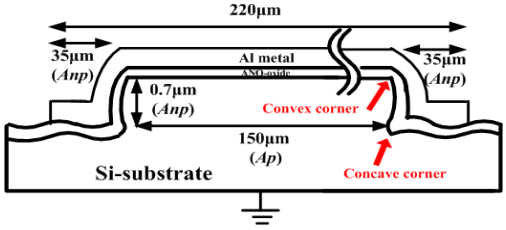

Fig. 1.The cross section of non-planar MOS device with thin oxide grown by anodic oxidation.

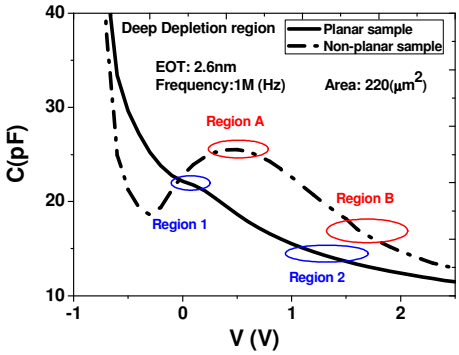

Fig. 2. Deep depletion characteristics of planar and non-planar devices.

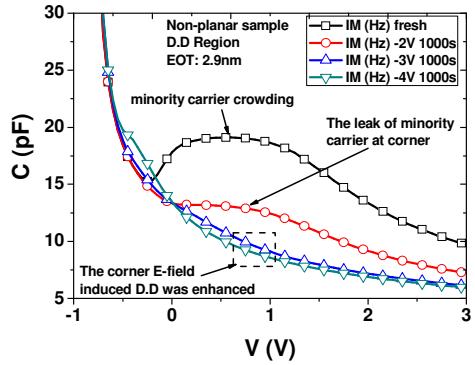

Fig. 3. The deep depletion behavior of non-planar device after CVS.

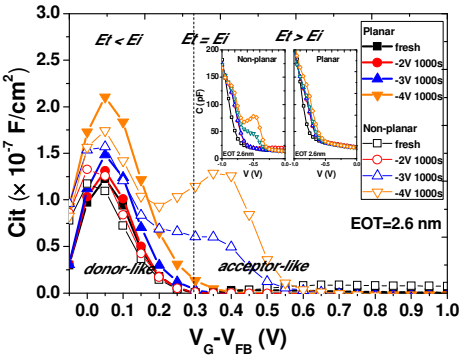

Fig.4 . The C_{it} versus V_G-V_{FB} curves of (a) non-planar and (b) planar samples after consecutive negative constant voltage stresses.