Transfer-free Bilayer Graphene FETs: Application as Memory Devices

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Introduction

In this paper we report on the application of in-situ CCVD grown bilayer graphene transistors (BiLGFETs) as memory devices. By means of catalytic chemical vapor deposition (CCVD) the BiLGFETs are realized directly on oxidized silicon substrate without transfer. These BiLGFETs possess unipolar p-type device characteristics with a high on/off-current ratio between 1×10^5 and 1×10^7 at room temperature [1, 2]. The hysteresis of BiLGFETs depends on the cycling range of the applied backgate voltage V_{BG} while the sub-threshold slope is uniform for varied temperatures and varied cycling ranges of the backgate voltage [3]. Based on the observed properties of BiLGFETs it is possible to use BiLGFETS as memory devices.

Fabrication of BiLGFETs

In preparation for CCVD a silicon wafer is oxidized in dry O_2 ambient to obtain a 100nm thick SiO₂ film. Afterwards several lithography steps follow and a structured liftoff system remains on the wafer surface. Thin aluminum and nickel layers are evaporated over the whole substrate surface and are structured via liftoff. By annealing the wafer the aluminum transforms itself into insulating aluminumoxide (Al_xO_y) while the nickel layer generates several nickel nanoclusters at the perimeter of the catalyst system [1, 2]. In the subsequent methanebased CCVD process, graphene layers are growing while the number of the stacked graphene layers depends on the adjusted process parameters like time, temperature and gas mixture [3].

Results and Discussion

The electrical characterization of the transistors is performed using a Keithley SCS 4200 semiconductor characterization system. The catalyst pads are used as source and drain contacts. Figure 1 shows the current voltage characteristic of a BiLGFET as a function of the applied backgate voltage (V_{BG}) showing an on/off-current ratio of 1x10⁵ at room temperature. V_{BG} is swept from -10V to 10V and reverse. In this case the hysteresis of the BiLGFET is ΔV_{BG} = 11V and is most likely based on the trapping and detrapping of oxide charges from the backgate oxide [3].

The band structure of BiLG is known to be sensitive to the lattice symmetry. Provided that the two graphene layers generate an asymmetric double layer, an energy gap forms at the former Dirac crossing points [4]. Accordingly, the bandgap of an asymmetric double layer can be further enhanced by means of graphene/substrate interfacial interactions [5], and does not originate from an applied electrical field in this case. Since there is a permanent bandgap, the Schottky-barriers at the graphene/metal contact needs to be taken into account. The applied backgate voltage is used to affect the Schottky-barrier at the source/drain to graphene contacts, thereby switching the BiLGFET on and off.

To store a logical "1" a backgate voltage of V_{BG} = 10V is applied. In contrast to this a logical "0" is written by applying a backgate voltage of V_{BG} = -10V. The stored information can be read at V_{BG} = 0V. Figure 2 shows a

cycle of writing and reading. At first a logical "0" is written. Reading at V_{BG} = 0V results in a S/D current of I_{DS} ~10⁻¹²A. Ongoing a logical "1" is written and the subsequent reading provides a current value of I_{DS} ~10⁻⁷A. The storage of a logical "0" or "1" is repeatable and reproducible (Fig 2). Several cycles of writing and reading have been realized without any observable degradation of the device performance.

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References

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Figure 1: Current-voltage characteristics of a bilayer graphene transistor with hysteresis as a function of the applied backgate voltage V_{BG} exhibiting an on/off-current ratio of 1×10^5 at room temperature. V_{BG} is swept from - 10V to 10 V and reverse.



Figure 2: Repeatable and reproducible storage of logical "0" and "1" current levels as a function of time. By applying $V_{BG} = -10V$ (+10V) a logical "0" ("1") is written. When measuring I_{DS} at $V_{BG}=0V$ yields the information if a logical "0" or "1" has been stored.