# Impact of Disturb on Retention Time in Single FBRAM Cells

S. D. dos Santos[1], T. Nicolleti[1], J.A. Martino[1],
M. Aoulaiche[2], M. Jurczak[2], E. Simoen[2] and C. Claeys[2,3]
[1]LSI/ PSI/USP - University of São Paulo, SP, Brazil
[2]imec, Leuven, Belgium
[3]E.E. Dept., KU Leuven, Leuven, Belgium

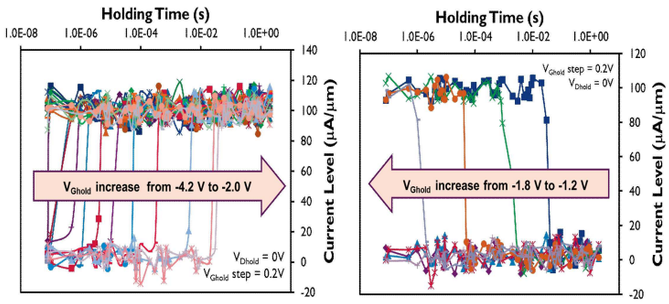
One of the possible applications for Ultra-thin Buried Oxide (UTBOX) MOSFETs has been as a capacitor-less Floating-Body RAM (FBRAM) cell. The most attractive feature in this case is the fact that the charges are stored in the body of the transistor, avoiding the necessity of the capacitor that occupies a large area in the cell (1-3). But in a matrix transistor integration, an important behavior must be evaluated to determine its functionality: the Word line (WL) and the Bit line (BL) disturbs (4). The disturb analysis shows the impact of the BL/WL polarization on the storage data recorded in a transistor body. To access one specific transistor implies biasing the other ones which are connected to the same BL and WL. As a consequence, the data (bit 0 or bit 1) previously recorded in those transistors can be lost or disturbed. In this work, the retention time is studied in order to verify the influence of the WL and BL voltage disturb on the stored data i.e. "0" and "1" states. According to the operation windows established in these cases, the writing "0" biases are optimized to minimize the disturb.

The nMOSFETs were fabricated on 300mm diameter Silicon-On-Insulator (SOI) wafers with silicon and box thickness of around 14nm and 18nm, respectively. The gate stack consists of 5nm plasma enhanced atomic layer deposition (PEALD) TiN capped with 100nm a-Si deposited on a 5nm-thick thermal $SiO_2$. 20nm-wide nitride spacers and a P-only HDD implantations resulted in extensionless structures with Si-epitaxial raised Source-Drain (SEG). The effective channel length (L) is 95nm and the channel width is 1µm. All analyzes are performed at 85ºC.

Based on the biasing scheme applied in (3,5) with a back-gate bias $V_B$=3.3V, the conventional holding conditions correspond to $V_{Ghold}$=-2.5V and $V_{Dhold}$=0V. Figure 1a shows the state "0" and "1" current level as a function of the holding time obtained for $V_{Dhold}$=0V and different gate bias between a write and a subsequent read, varying from -4.2V to -2.0V. For all the conditions presented in figure 1a, the state "0" is disturbed due to holes generation originated by GIDL. Because of that, higher gate biases decrease this effect and improve the retention time (3). On the other hand, by increasing $V_{Ghold}$ from -1.8V to -1.2V, as presented in figure 1b, one can notice the decrease of the retention time and the disturb of the state "1". For more positive gate bias, the accumulated charges tend to decrease, resulting in the loss of holes which reduces the current level to the OFF-state.

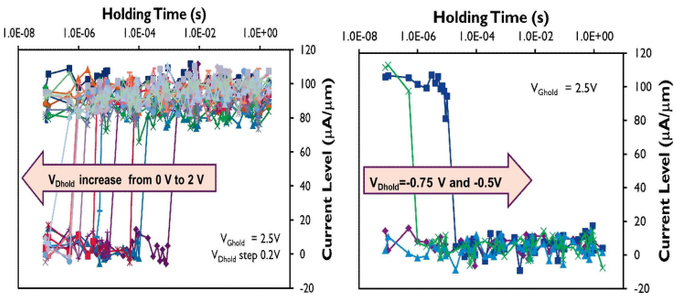
From figures 2a and 2b, it is possible to observe the influence of BL disturb on the retention time. In this case the BL holding bias between a write and read is varied from -0.75V to 2V while the WL holding bias is kept constant and equal to -2.5V. Two cases are observed as previously for WL disturb. High BL bias is responsible for hole generation which disturb the state "0", by changing the current level to the ON-state. However, negative BL bias disturb opens the body/drain junction and the holes are removed (state "1" is disturbed).

Figures 3a and 3b show the worst case retention time as a function of the WL and BL bias disturb, respectively. The usual holding condition is highlighted in order to compare it with the other biases as well as the optimum retention time situation.




State "0" is disturbed (a) State "1" is disturbed (b)

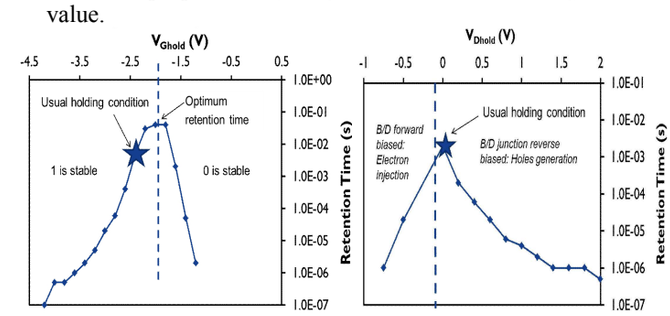
Figure 1. State "0" and "1" currents as a function of the holding time for increased word line holding bias between a write and a subsequent read, showing the ON-state (a) and the OFF-state disturb (b).




State "0" is disturbed (a) State "1" is disturbed (b)

Figure 2. State "0" and "1" currents as a function of the holding time for increased bit line holding bias between a write and a subsequent read for positive (a) and negative drain biases (b).

According to figure 3a the greater retention time of about 40ms is obtained for WL holding bias of -2V, which is 8 times higher than the one obtained at the usual $V_{Ghold}$. For a WL bias disturb higher or lower than -2V the retention time is decreased. Beside, in the case of the BL bias, the retention time is optimum for no BL disturb (0V) and it is proportionally degraded to the disturbing bias value.




(a) (b)

Figure 3. Worst case disturb retention time versus the word line disturb bias ($V_{Ghold}$) (a) and the bit line disturb bias ($V_{Dhold}$) (b).

Based on the range of WL and BL disturb on the retention time, it was determined a writing "0" condition to operate avoiding the region of disturb. The previously reported writing "0" condition based on (3,4) consists of a $V_D$=0.5V and $V_G$=-0.5V. For reduced disturb it was found that more negative $V_G$ can be used with slightly higher or negative $V_D$, presenting no significant impact on the $V_{GREAD}$ and on the retention time.

**References**

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