# Deposited ALD $SiO_2$ HKMG Interface for High Voltage (HV) Analog and I/O Devices on Next Generation Alternative Channels and FINFET (3D) Device Structures

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Gate oxides have traditionally used thermally grown $SiO_2$ gate oxide for high voltage I/O devices. Although this process creates a highly reliable gate oxide or interlayer oxide, it consumes the channel silicon. Therefore, due to channel consumption, thermally grown $SiO_2$ is not feasible with either a SiGe channel device, or FinFET and ETSOI technologies.

In this paper, we compare low temperature (T< 800 $^oC$) CVD deposited $SiO_2$, organometallic ALD $SiO_2$ with post nitridation and anneal process, and thermally grown $SiO_2$ in terms of process, device, and reliability. The optimized ALD $SiO_2$ has been incorporated in a 32 nm HKMG technology and is extendable to both ETSOI and FINFET architectures for SOC applications.

To replace the thick thermal $SiO_2$ layer both CVD and ALD $SiO_2$ were evaluated. Initially CVD $SiO_2$ was evaluated, but the limitations of this process are many. CVD $SiO_2$ within wafer thickness non-uniformity is large on 300 mm wafers. CVD $SiO_2$ process is also not capable of conformal deposition which leads to thinner oxide at the edge of shallow trench isolation (STI). Due to these CVD process issues, degradation in reliability and non-uniformity is apparent in the TDDB Weibull plot (Fig.1) where four capacitors with different areas violate Poisson area scaling. In summary, due to poor process control, non-conformality, and dielectric reliability, CVD $SiO_2$ is not a viable candidate for thick oxide based I/O devices.

For ALD $SiO_2$, deposition temperature is optimized to alter the incorporation of GeO from SiGe channel into the deposited oxide. The optimized higher temperature ALD process also has < 0.5% within wafer thickness non-uniformity. In addition, ALD deposition is conformal, and deposits a uniform thickness across STI edge region. The TDDB Weibull distribution (Fig. 2) exhibits well behaved Poisson area scaling with all the four different areas lining up, indicating no edge thinning. Although the ALD process is uniform there is a differential growth rate between pFET (cSiGe) and nFET (cSi) 7 Å – 10 Å Tinv difference. Optimizing the SiGe surface passivation before ALD deposition minimizes the differential growth rate yielding an acceptable 2.9 Å Tinv difference. Tinv delta minimization will also be crucial to enable I/O devices for potential future dual channel FINFET architectures.

Optimized nitrided ALD $SiO_2$ follows the VBD-Tinv trend of thermal oxide (Fig. 3) and we demonstrate that it has similar or better TDDB reliability compared to a thermal oxide, demonstrating the viability of the ALD $SiO_2$ process. TEM images of ALD $SiO_2$ I/O devices show atomically smooth interfaces with Si and SiGe layer (Fig. 4). The optimized ALD oxide has been extended to FINFET architecture (Fig. 5), creating thick oxide devices required for SOC applications.

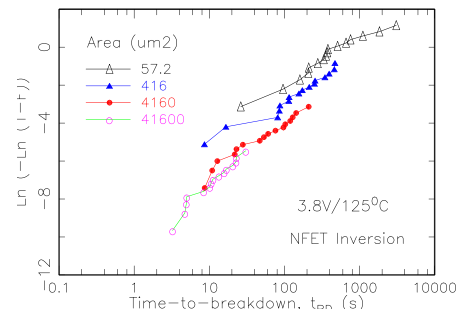


Fig 1: Weibull Plot of CVD $SiO_2$ oxide break down from four capacitors with different area illustrating non-Poisson area scaling, and extrinsic degrade

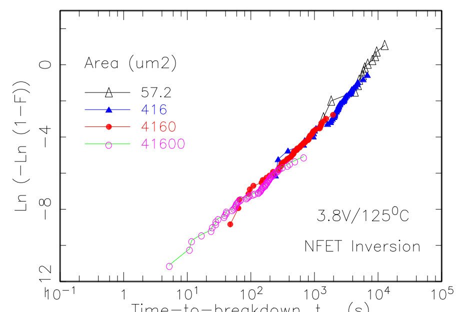


Fig 2: Weibull Plot of ALD $SiO_2$ breakdown from four capacitors with different areas illustrating Poisson area scaling

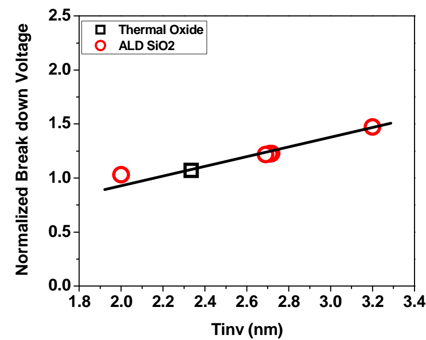


Fig 3: Normalized breakdown voltage Vs Tinv for ALD $SiO_2$ and thermal oxide

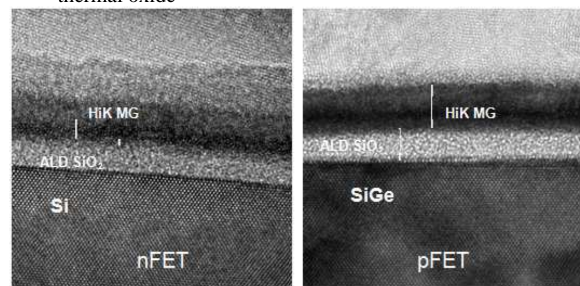


Fig 4: TEM of I/O nFET (Si-channel) and pFET (SiGe channel) showing the interface of channel-gate oxide with ALD $SiO_2$

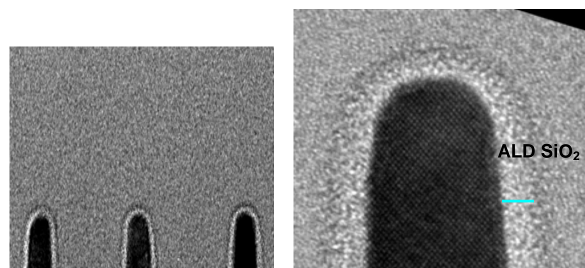


Fig 5: FinFET structure showing conformal deposited ALD $SiO_2$ as a thick oxide for I/O devices

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**Reference**

**[1]** S. Krishnan et al, IEDM, pp. 634 (2011)