Limiting factors of channel mobility in III-V/Ge MOSFETs

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MOSFETs using III-V/Ge channels with high mobility and low effective mass have been regarded as strongly important for obtaining high current drive and low supply voltage CMOS under sub 10 nm regime [1, 2]. Thus, the development of the device technologies for III-V/Ge MOSFETs has been strongly accelerated. However, fundamental device physics on electrical properties of III-V/Ge MOSFETs has not been fully clarified yet. Among a variety of the electrical properties, understanding of limiting factors of the III-V/Ge MOS channel mobility is of paramount importance, because the purpose of introducing these devices consists in the high current drive. In this paper, thus, we address key issues for enhancing channel mobility in InGaAs/Ge MOSFETs.

It is well known that superior MOS interface properties can provide higher channel mobility, because of reduction in Coulomb scattering and surface roughness scattering. We have confirmed in Ge p-MOSFETs with ultrathin GeO_x interfacial layers formed by plasma post oxidation [3], as shown in Fig. 1, that the GeO_x thickness can control the peak mobility in a low N_s region [4]. This fact is attributed to lower D_{it} near E_v, estimated from the S factor, in thicker GeO_x, as shown in Fig. 2. On the other hand, we have recently found [5] that the hole mobility in Ge p-MOSFETs in a high N_s region is significantly degraded by both trapping of free holes and severe surface roughness scattering. Thus, further reductions in MOS interface defect concentration and interface roughness are expected to provide higher mobility.

We have reported through Hall measurements [6] that the trapping of free electrons into interface states or slow states within the conduction band also significantly lowers electron mobility in InGaAs MOSFETs. In addition, another critical factor for the electron mobility reduction is the influence of the ultrathin body channels, which are mandatory for short channel MOSFETs. It has been reported that ultrathin Si channels severely reduce the channel mobility, because of increased body thickness fluctuation scattering [7]. This thickness fluctuation scattering becomes worse for III-V MOSFETs with lower effective mass and wider inversion-layer thickness. Thus, we have proposed MOS interface buffer channel structure, where InGaAs buffer layers sandwich InGaAs channels with higher In content [8]. This structure is expected to allow us to mitigate the influences of MOS interface defects and the channel thickness fluctuation. Actually, we have observed the significant mobility enhancement in the $In_{0.3}Ga_{0.7}As/In_{0.7}Ga_{0.3}As/In_{0.3}Ga_{0.7}As$-OI structure over single $In_{0.7}Ga_{0.3}As$-OI structures. The mobility was evaluated with changing the thickness of the channel and the buffer (Fig. 4). It is found that thickness fluctuation scattering and surface roughness scattering dominate the mobility in low and high N_s region, respectively.

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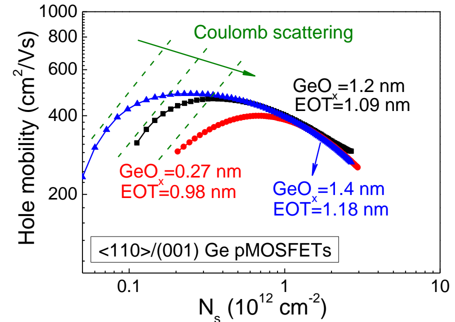

Fig. 1 Mobility of Ge pMOSFETs with the $Al_2O_3/GeO_x/Ge$ gate stacks having different GeO_x ILs thicknesses.

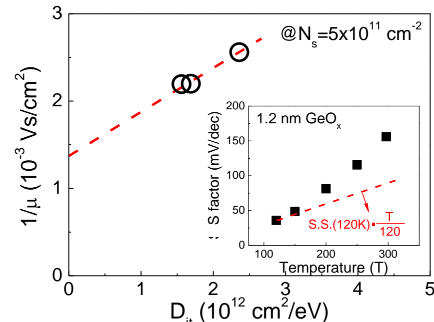

Fig. 2 The mobility of Ge pMOSFETs with $Al_2O_3/GeO_x/Ge$ gate stacks (@N_S=5×10^{11} cm^{-2}) as a function of D_{it} evaluated from the S. S. factors measured at 120 K. Inset t shows the temperature dependence of S factor.

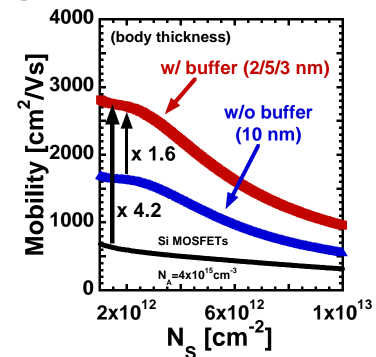

Fig. 3 μ_{eff} characteristics of $In_{0.7}Ga_{0.3}As$-OI MOSFETs with and without MOS interface buffer.

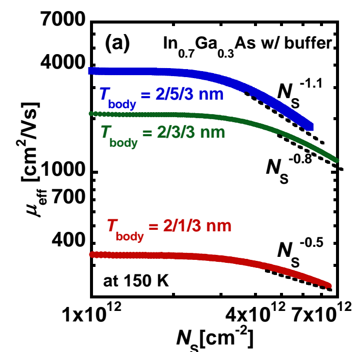

Fig. 4 μ_{eff} characteristics of $In_{0.7}Ga_{0.3}As$-OI MOSFETs with a MOS interface buffer layer as a parameter of the T_{body} at 150 K

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