III-V/Ge CMOS device technologies for high performance logic applications

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MOSFETs using channel materials with low effective mass have been regarded as strongly important for obtaining high current drive and low supply voltage CMOS under sub 10 nm regime [1, 2]. From this viewpoint, attentions have recently been paid to III-V and Ge channels. This is because III-V semiconductors have extremely high electron mobility and low electron effective mass and Ge has extremely high hole mobility and low hole effective mass. Thus, one of the ultimate CMOS structures can be the combination of III-V nMOSFETs and Ge pMOSFETs [1-4].

In order to realize III-V/Ge CMOS, common gate stack and S/D formation technologies are important. Here, an ALD Al_2O_3 gate insulator and Ta metal gate were used for common gate stacks for InGaAs and Ge. This is because ALD Al_2O_3 can provide good MOS interfaces with InGaAs as well as Ge with post ECR plasma oxidation [5]. Also, self-align Ni-Ge and Ni-InGaAs [6], which can be formed simultaneously for InGaAs nMOSFETs and Ge pMOSFETs, were used as the metal source/drain (S/D) regions.

By utilizing these technologies, we have demonstrated successful integration of InGaAs-OI nMOSFETs and Ge p-MOSFETs on a same wafer and their superior device performance [7]. In order to realize the integration of III-V/Ge MOSFETs and examine the feasibility of proposed integration processes, we have bonded III-V substrates with Ge substrates as a preliminary work. InGaAs-on-Ge wafers with 20-, 50-, and 100-nm-thick InGaAs layers were fabricated for integrating InGaAs-OI nMOSFETs and Ge pMOSFETs. The process flow and the fabricated device structure are shown in Fig. 1. Here, we used the Al_2O_3 BOX layer with plasma post oxidation as the gate-insulator for Ge pMOSFETs. Ni-based metal S/D for both InGaAs and Ge was formed by annealing at 250 ºC for 1 min. We have confirmed that the Ni-InGaAs and Ni-Ge metal S/D are successively formed with Ta gate. The top view of the fabricated devices is shown in Fig. 2.

We have found good transistor operation in both devices, shown in Fig. 3, High I_{on}/I_{off} ratio of ~10^6 was obtained for InGaAs-OI nMOSFETs. The high electron and hole mobility of 1800 and 260 cm^2/Vs and the mobility enhancement against Si of 3.5× and 2.3× have been demonstrated for InGaAs-OI nMOSFETs and Ge pMOSFETs, respectively, as shown in Fig. 4.

While the present devices still have thick EOT because of the single Al_2O_3 gate insulator, we have recently realized HfO_2/Al_2O_3 gate stacks with EOT of 1 nm or less for both InGaAs [8] and Ge [9], allowing us to simultaneously satisfy both thin EOT and good MOS interface properties as the common gate stacks.

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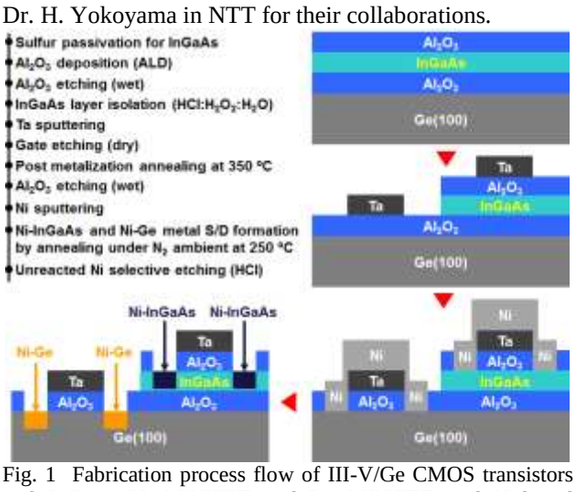

Fig. 1 Fabrication process flow of III-V/Ge CMOS transistors with InGaAs-OI nMOSFETs and Ge pMOSFETs with Ni-based metal S/D on the InGaAs-OI-on-Ge wafer

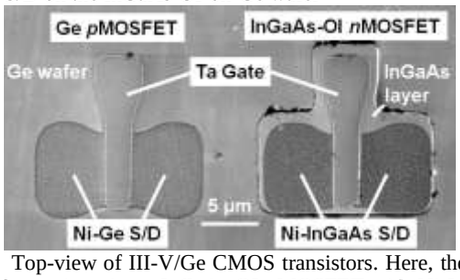

Fig. 2 Top-view of III-V/Ge CMOS transistors. Here, the right and left transistor is an InGaAs-OI nMOSFET with Ni-InGaAs S/D and a Ge pMOSFET with Ni-Ge S/D, respectively

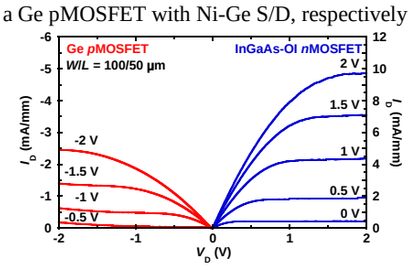

Fig. 3 $I_D - V_D$ characteristics of a Ge pMOSFET and a 20-nm-thick InGaAs-OI nMOSFET.

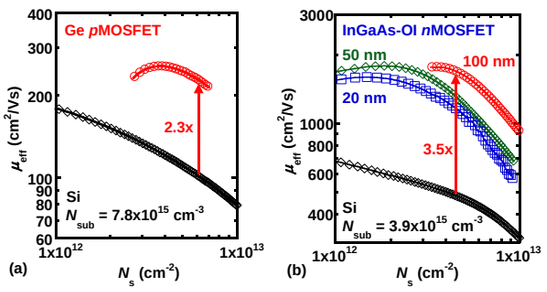

Fig. 4 $\mu_{eff} - N_s$ characteristics of (a) Ge pMOSFETs and (b) InGaAs-OI nMOSFETs with InGaAs-OI channel layer thickness of 20, 50, and 100 nm. The InGaAs-OI nMOSFETs show higher electron mobilities than Si MOSFETs regardless of InGaAs-OI channel layer thickness.

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