Atomic Scale Thickness Control of SOI Wafers for Fully Depleted Applications

W. Schwarzenbach, N. Daval, V. Barec, O. Bonnin,
P. Acosta-Alba, C. Maddalon, A. Chibko, T. Robson,
B.-Y. Nguyen & C. Maleville
SOITEC – F-38190 Bernin – France

SUBSTRATE REQUIREMENTS

Smart Cut® Technology has recently been moved forward to a performance that seemed impossible until just recently. FDSOI requirements demand a method to transfer an ultra-thin crystalline layer with near perfect uniformity. Silicon thickness variation across all wafers has been improved by a factor of 10, while at the same time roughness was decreased by factor of 5. BOX is available over a wide range of thicknesses from 10 to 50nm ready to satisfy all possible applications, and next generation strain silicon layer is in advanced development stages to prepare for future nodes. Such development efforts has now been materialized in process technology qualification [1] and proven for further node scaling.[2] This paper reports the latest achievements in state of the art thickness and roughness control, which is enabling very low variability fully depleted technologies today.

WAFER SCALE THICKNESS VARIATION ACHIEVEMENT

Making ultra-thin SOI & BOX (UTBOX) substrates requires near-perfect oxidation conditions and optimized implant & splitting anneals in the conventional Smart Cut process. On-wafer SOI thickness uniformity down to 3 A peak to peak has been demonstrated, in addition to tight wafer to wafer control through APC (Advance Process Control).[3] It allows volume production of 12nm SOI / 25nm BOX substrates with wafer scale SOI thickness maximum variation of +/- 5 A (6 sigma value, all sites, all wafers) as shown on Fig. 1.[4]

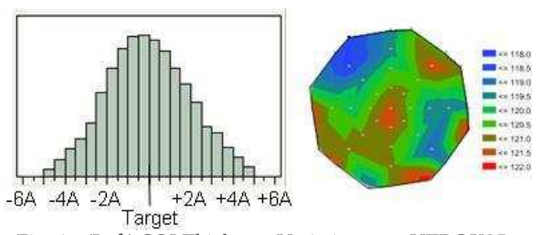

Fig. 1 : (Left) SOI Thickness Variation over UTBOX25 manufacturing volume. (Right) 3 A SOI thickness range wafer on 41pts ellipsometry mapping.

DEVICE SCALE THICKNESS VARIATION IMPROVEMENT

Device scale thickness variation is monitored through micro-roughness performance. In addition to previously mentioned conventional Smart Cut process step optimizations, several finishing options have been evaluated, aiming to reduce final SOI surface roughness while keeping excellent on-wafer SOI uniformity.

The use of Chemical-Mechanical-Polishing processes allow excellent roughness performance but currently induces significant on-wafer SOI uniformity degradation, even with limited Si removal. Fig .2 shows the typical tradeoff between roughness & on-wafer uniformity.

Thermal smoothing through the surface diffusion process as described by Mullins-Herring surface diffusion equation,[5] allows reducing surface roughness with a limited impact on wafer-scale SOI uniformity. Fig.3 shows, for a given process temperature, the impact of soak duration on SOI roughness as measured by Power Spectral Density (PSD) on a 30x30 µm^2 AFM scan.

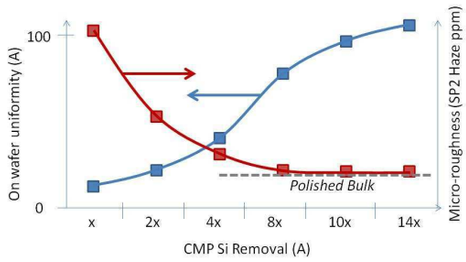

Fig.2 : On-wafer uniformity & Micro-roughness measured through SP2 Haze *vs* CMP Si removal

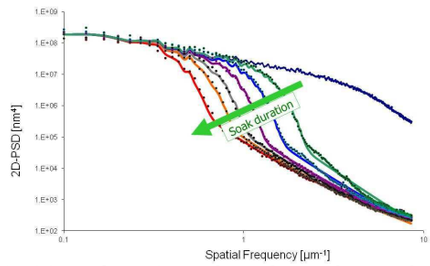

Fig.3 : SOI surface PSD *vs* thermal smoothing soak duration

Fig. 4 shows AFM results on several UTBOX substrate options. In contrast to the ≥ 3 A 30x30 µm^2 RMS on Partially Depleted SOI products, UTBOX for Fully Depleted applications exhibit a 0.8 A 30x30 µm^2 RMS.

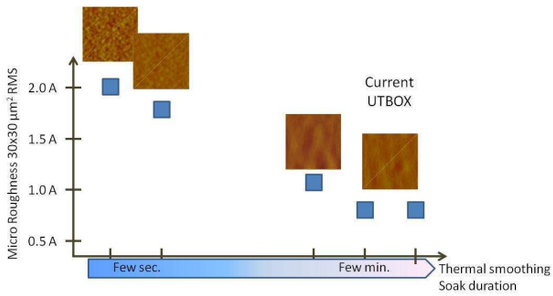

Fig. 3 : AFM micro-roughness performance

BOX THICKNESS CONTROL TO SUPPORT FD SCALING

These ultra-thin SOI substrates, designed for Fully Depleted Planar Technologies targeting 5 – 7 nm channel silicon thickness under the gate of the devices, are associated with an ultra-thin BOX layer of 25 nm, controlled within a 1 nm range to enable enhanced body bias behavior. These substrates are now in production.

BOX thickness reduction to 10 nm has been developed using the Smart Cut process combined with BOX dissolution of high temperature annealing. [6]

SOI thickness can be easily adjusted to meet channel thickness requirement for electrostatic control. BOX reduction will also contribute to FD scaling path due to improved electrostatic control via the back gate.

REFERENCES

[1] N. Planes *et al*, VLSI Symp. 2012
[2] A. Khakifirooz *et al*, VLSI Symp. 2012
[3] W. Schwarzenbach *et al*, ICICDT 2011
[4] W. Schwarzenbach *et al.*, ECS Trans., vol. 45, p.227, 2012
[5] O.Kononchuk *et al*. The 6th Int. Symp. on Advanced Science and Technology of Silicon Materials, 2012
[6] O. Kononchuk *et al*, Solid State Phen., vol 156, p.69, 2009