The Generation Rate Analysis of Different S/D Junction Engineering in Scaled UTBOX 1T-DRAM

T. Nicoletti[1], K.R.A. Sasaki[1], S.D. dos Santos[1], J.A. Martino[1], M. Aoulaiche[2], E. Simoen[2] and C. Claeys[2,3]

[1]LSI/ PSI/USP - University of São Paulo, SP, Brazil
[2]imec, Leuven, Belgium
[3]E.E. Dept., KU Leuven, Leuven, Belgium

Recently, a new concept of a capacitor-less 1-transistor dynamic memory cell called (1T-DRAM) has been developed. This new memory cell exploits the floating body where the transistor body is used as a charge storage node (1-2). One of the biggest issues is its retention time that scales together with the gate length of the cell (3-4). In order to overcome this issue, different source/drain engineering is used combined with UTBOX technology, showing an advantageous way of improving the device performance (5-6). In this work, based on experimental data and confirmed by simulation results, the retention time degradation with the channel length is demonstrated, as well as its correlation with the electric field, gate-induced-drain-leakage (GIDL) and the generation rate by band-to-band-tunneling. The UTBOX FDSOI devices were built on 300-mm diameter SOI wafers with t_{si} and t_{box} of ~18 and ~14-nm, after the device processing. The standard junctions were defined by low-energy As-implantation extensions, followed by 30nm-wide nitride-spacers formation while the underlap junctions were defined with 20nm-wide nitride-spacers. Devices with effective channel lengths (L) varying from 30 to 215nm were investigated. The measured devices were modelled using 2D numerical simulations (7). All the analyses were performed at 85ºC and more process information can be found in (4). Figure 1 demonstrates the electric field behavior along the channel length.

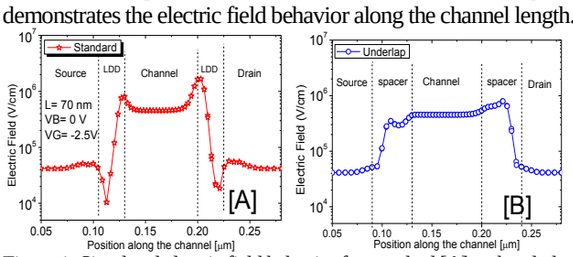

Figure 1: Simulated electric field behavior for standard [A] and underlap [B] S/D junctions.

It is known that the electric field is L dependent and in this case about two times higher for standard S/D junctions. Another important thing to point out is that the misalignment of the peaks between the devices occurs due to the presence of the LDD region in the standard device while in the underlap one it changes abruptly from S/D to the undoped region. With the programming scheme used in this work (4), the retention time is determined by the state-0 degradation, the increase of the off-state current, i.e. hole generation. Therefore the lateral field impact is expected to be lower since the studied devices have a lowly doped Si film and the effects are further reduced for underlap ones. Figure 2A shows the 1T-DRAM retention time as a function of L for standard and underlap devices through experimental results.

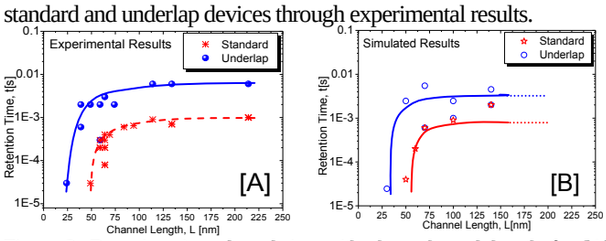

Figure 2. Retention time degradation with short channel length for [A] experimental and [B] simulated results.

The same analysis was reproduced by the simulations of figure 2B confirming the retention time degradation for short channel lengths. The mechanism behind the degradation is attributed to the GIDL current amplification by the lateral bipolar transistor with narrow base. In order to validate the experimental results, figure 3 presents the simulated generation rate along the channel near the front interface and figure 4, along all the structures, for the best scaled channel length with the best back bias condition for each technology.

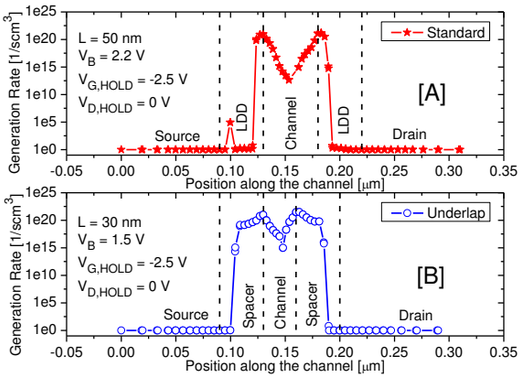

Figure 3: Generation rate along the channel during the holding-0 at 1nm below the first interface for the shortest channel length of standard [A] and underlap [B] S/D junctions technology.

From figure 3, it is possible to see a similar generation rate near the junctions for these devices. However, this was achieved using a lower back bias which increases the retention time. These behaviors follow the same tendency as the experimental results and match with figure 2B, since the retention time of standard and underlap devices are also close, 0.2ms and 0.14ms, respectively. Simulations indicated that the main effect acting to the electron-holes pairs generation is the GIDL, as can be seen through figure 4, where higher generation rates near the junctions are present only when the BTBT model was considered [A]. This demonstrates a better downscaling for the underlap devices, since the shortest channel lengths of each technology can reach closer retention times. Another advantage using underlap is the lower back biases applied.

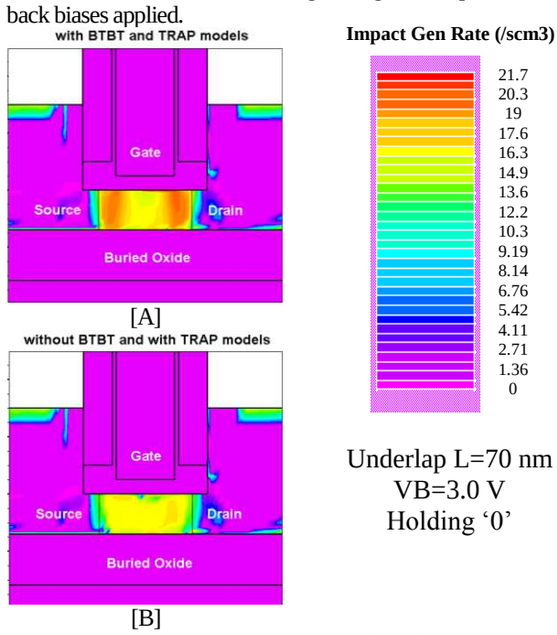

Figure 4: Generation rate along the channel for underlap S/D junctions during holding-0, with the BTBT model [A] and without it [B].

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