Influence of high temperature on UTBB SOI nMOSFETs with and without ground plane

V. Sonnenberg[1,2], V. Itocazu[1], J. A. Martino[1], E. Simoen[3], C. Claeys[3,4]

[1]LSI/PSI/USP, University of Sao Paulo, SP, Brazil
[2]FATEC, Faculdade de Tecnologia, Sao Paulo, Brazil
[3]Imec, Leuven, Belgium
[4]E.E. Dept., KU Leuven, Belgium

The Fully Depleted (FD) SOI MOSFET with Ultra Thin Body and Buried Oxide (UTBB) is considered as one of the best candidates for sub 28nm technology nodes due to the better short channel effect (SCE) maintaining the well known planar structure (1). However for thinner buried oxide the coupling between the front and back gate becomes stronger and amplifies the substrate effects as first modeled in ref. (2). For UTBB transistors the substrate effect becomes even worse and due to that it is mandatory to have a Ground Plane (GP) implantation (at the buried oxide/substrate) in order to minimize/avoid the depletion region at the buried oxide/substrate interface, which is the reason of the substrate effects. This paper studies experimentally and by numerical simulation the temperature influence on UTBB devices with and without GP implantation.

The UTBB SOI nMOSFET devices studied were fabricated in a SOI substrate with 6nm and 14nm Si film on 18nm buried oxide. The gate dielectric consists of a 5nm SiO_2 thermal oxide, followed by a TiN metal gate electrode. No channel doping was applied so that the doping level of the channel is around 10^{15} cm^{-3}. The Ground Plane was done with a boron implantation at 25keV and $5x10^{13}$ cm^{-2}. Two different L, 10µm and 70nm, was measured with W=1µm.

Figure 1 shows the experimental drain current vs. back gate voltage (I_{DS} vs.V_{GB}) curves with V_{GF}=0V, V_{DS}=50mV, t_{Si}=6nm, L=10µm and W=1µm for 25°C, 100°C and 200°C for devices with and without GP implantation, where it is possible to see a back gate voltage shift (kink) for devices without GP. This effect disappears for devices with GP substrate doping concentration higher than 10^{18} cm^{-3} as observed in ref. (3). For high temperature, this effect occurs for almost the same back gate voltage, but the maximum amplitude ($\Delta V_{GB\ MAX}$) decreases as shown in figure 2 due to the Fermi level reduction. Figure 2 also shows that for a thinner silicon film the substrate effect is lower due to the stronger influence between the front and back gates. The same tendency was observed for shorter devices with L = 70 nm, but lower $\Delta V_{GB\ MAX}$ was obtained due to SCE.

Numerical simulation (4) was used in order to analyze the potential drop along the SOI structure with V_{GF}=0 and V_{GB}= -0.2V and 1V at T=25°C and 200°C, as presented in figure 3. UTBB SOI nMOSFETs with a substrate doping concentration of $Na_{SUB}=10^{18}$ and 10^{15} cm^{-3} were used to simulate devices with and without GP respectively. The substrate potential drop (Φ_{sub}) for V_{GB}= -0.2V, when the buried oxide/substrate interface is near inversion, is almost zero for GP devices while it is around 0.7V for devices without GP. However, figure 3b shows that in spite of $\Phi_{sub} \approx 0$ the potential inside the buried and gate oxide is higher for GP devices which can cause reliability problems. For high temperature the Fermi level decreases and the Φ_{sub} decreases to 0.3V for devices without GP at 200 °C.

As a conclusion, in spite that GP devices present negligible substrate potential drop, the impact on SOI devices becomes higher, increasing the potential drop at the buried and gate oxide, which can cause early degradation. When the temperature increases the substrate effect decreases and devices without GP can be useful for some special applications. Other electrical characteristics will be presented in the extended version.

References

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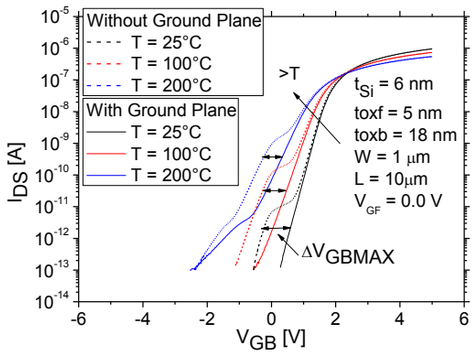

Fig. 1 – Experimental drain current vs. back gate voltage for UTBB devices with and w/o GP at different temperatures.

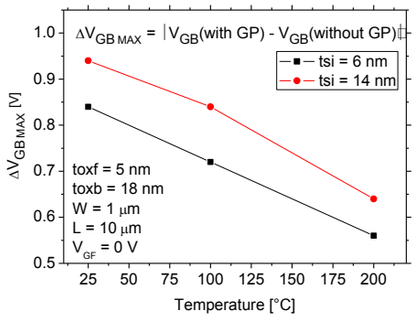

Fig. 2 – Experimental maximum voltage difference between the back gate voltage ($\Delta V_{GB\ MAX}$) in function of temperature for t_{Si}= 6nm and 14nm.

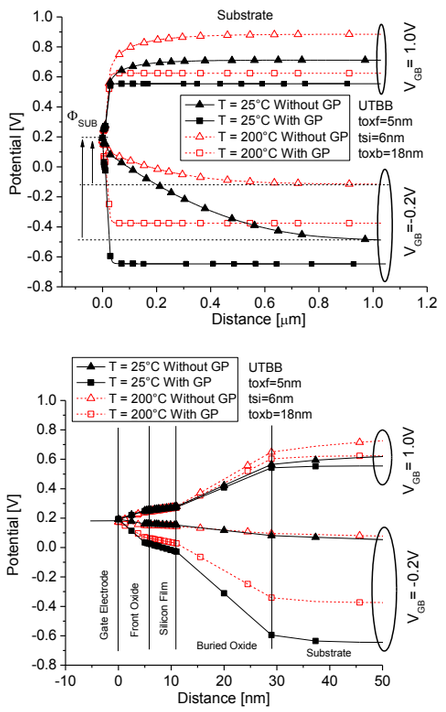

Fig. 3 – Potential simulation for V_{GF}=0 and V_{GB}=-0.2 and 1V comparing UTBB with and without GP for T=25°C and T=200°C, (a) from gate electrode (0) to 1.2µm and (b) the first 50nm.