Experimental comparison between pTFET and pFinFET under analog operation

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The multiple-gate field-effect transistors (MuGFET) emerged to allow higher scalability to MOSFET devices due to their better immunity to short-channel effects (SCE) (1). The triple gate FinFET has been studied in depth (1) for the 22 nm technology node. However, the predominant drift-diffusion transport mechanism limits the on-off switch behavior to 60 mV/dec at subthreshold regime. When the focus is the reduction of the supply voltage and consequently the dissipated power, which is mandatory for sub 22 nm nodes, the tunnel field-effect-transistors (TFET) appear as an alternative to replace the conventional MOSFETs due to their capability to reach a subthreshold swing smaller than 60mV/dec at room temperature (2). The focus of these studies has been the digital operation. Almost nothing about the analog behavior has been studied, exceptfor some preliminary simulations (3,4). In this work, an experimental comparative analysis between triple-gate pTFET and triple-gate pFinFET is performed from an analog point of view, for the first time.

Both types of devices (TFET and FinFET) were fabricated in the same wafer, using a horizontal FinFET technology. Both devices have the same characteristics, changing only the source implantation from p-type (for pFinFET) to n-type (for pTFET). The fin height is 65nm, the buried oxide thickness is 145nm, the gate is composed by 5nm TiN covered by a 100nm polysilicon layer and the gate dielectric consists of 2nm HfO_2 on a 1nm SiO_2. The analyzed devices have a channel length of 150nm and a fin width of 40 nm and 250nm. Further details can be found in (5).

Figure 1 shows the drain current (I_{DS}) behavior for pTFET and pFinFET for the same bias conditions. Figure 1A shows the I_{DS} currents as a function of gate voltage (V_{GS}) and figure 1B, the I_{DS} versus drain voltage (V_{DS}). From figure 1A it is possible to see that the pTFET device presents a low current drive capability when compared to the FinFET one, and the horizontal shift of the I_{DS} curve indicates that for devices with the same characteristics a higher $|V_{GS}|$ is necessary to onset the pTFET conduction. However, when the I_{DS} curves are analyzed as a function of V_{DS} (figure 1B) for $V_{GS}= -1.7V$, it is possible to observe that apparently both devices reach the "saturation region" (plateau) practically for the same drain voltage. The I_{DS} x V_{DS} curve also presents a horizontal shift, where the minimum I_{DS} (for pTFET) does not occur for $V_{DS}=0V$, as already observed in (6). It is caused by the gate current that is small but has the same order of magnitude as I_{DS} for this bias condition ($I_{DS}= 3.9$ pA).

The intrinsic voltage gain (A_V) is an important figure of merit to characterize the analog performance of devices. A_V was calculated by $A_V = gm/g_D$, where gm is the transconductance and g_D is the output conductance, both in saturation condition. The gm and g_D are presented in figure 2. Although gm for the pTFET is much lower than for the pFinFET, the influence of V_{GS} on gm is higher, reaching almost 2 orders of magnitude when $|V_{GS}|$ increases from 1.3V to 1.7V, due to the direct dependence of the tunneling current at the source/channel junction with gate bias. Focusing on the output conductance, a higher influence of V_{GS} on I_{DS} for pTFET can be also observed. However, the magnitude of g_D for pTFETs is almost 6 orders of magnitude smaller (better) than for pFinFETs. For $V_{DS}=-0.9V$ it is possible to notice a degradation of g_D because the I_{DS} curve for this drain bias does not reach a plateau.

As a result, although pTFET presents smaller gm, the strong g_D improvement obtained for this device results in a higher intrinsic voltage gain for all studied bias conditions as shown in figure 3.

It is know that a better performance of FinFET structures is obtained for narrow devices. However, when the analog behavior

was evaluated for a fin width of 40 nm at these bias conditions, as shown in table I, the self-heating effect (SHE) was observed for pFinFET devices with $|V_{DS}| \geq 1.2V$, and the comparison could not be done. Due to that, the comparison between pTFET and pFinFET for $W_{Fin} = 40nm$ was only performed for $V_{DS}= -0.9V$ which is not the best condition to evaluate the analog parameters for pTFETs. Even when the pTFET devices don't suffer from SHE, pTFETs still present an A_V increase of 77% for $V_{GS}= -1.7V$ and 48.5% for $V_{GS}=-1.3V$.
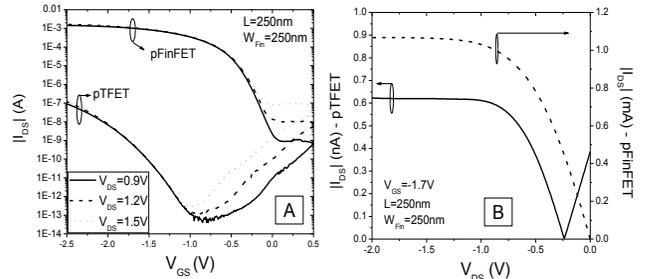

Figure 1: Drain current for pTFET and pFinFET devices as a function of gate bias (A) and drain bias (B).
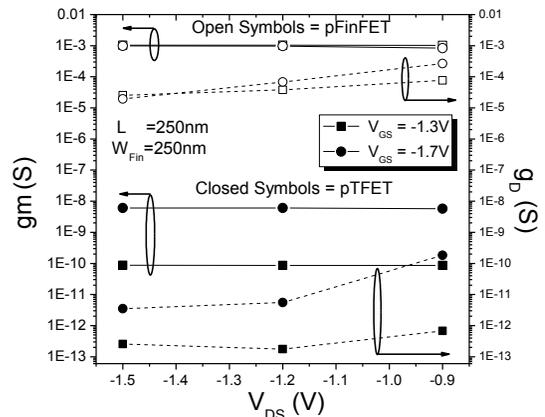

Figure 2: Transconductance and output conductance for pTFET and pFinFET varying the gate and drain bias.
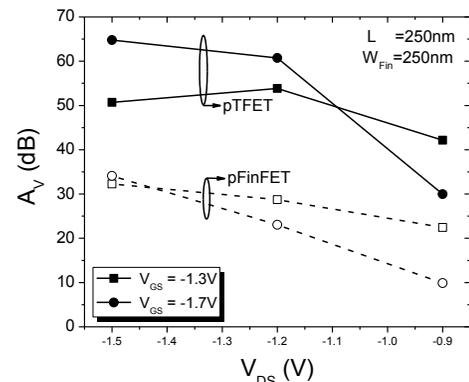

Figure 3: Intrinsic Voltage gain for different gate and drain bias for both device types (TFET and FinFET).

Table I: A_V (dB) for $W_{Fin} = 40nm$ and L=250nm.

	pTFET		pFinFET	
V_{DS} (V)	$V_{GS}=-1.3V$	$V_{GS}=-1.7V$	$V_{GS}=-1.3V$	$V_{GS}=-1.7V$
-0.9	55.16	18.73	31.13	12.61
-1.2	63.91	38.98	*	*
-1.5	80.88	80.94	*	*

* Self-Heating Effect (SHE).

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