Abstract #891, 223rd ECS Meeting, © 2013 The Electrochemical Society

Comparative Experimental Study Between Tensile and Compressive Uniaxially Stressed nMuGFETs under X-Ray Radiation focusing on Analog Behavior

V. V. Peruzzi[1], S. P. Gimenez[1,2], P. G. D. Agopian[1,2], M. A. G. Silveira[1], J. A. Martino[2], E. Simoen[3] and C. Claeys[3,4]

[1]FEI, Sao Bernardo do Campo, Brazil
[2]LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
[3]Imec, Leuven, Belgium
[4]E.E. Dept., KU Leuven, Leuven, Belgium

Introduction

Notwithstanding that planar Silicon-On-Insulator (SOI) Complementary Metal-Oxide-Semiconductor (CMOS) presents better single-event upset robustness than the bulk CMOS technology, thanks to the presence of a buried oxide (BOX) (1), it is less tolerant to the total ionization dose (TID) due to the generation of positive charges in the BOX region (2). Nowadays, the three-dimensional (3D) multi-gate SOI MOSFETs (MuGFETs) have been implemented in SOI technology in order to improve the current drive, short-channel effects (SCE) and TID tolerance (3). Besides, stress techniques have been using to improve the mobility and consequently the device performance (4). However, the influence of the radiation on stressed devices is less clear. This work aims to study experimentally tensile versus compressive uniaxially stressed triple-gate SOI MOSFETs fabricated on a tensile biaxial strained wafer (sSOI) submitted to an X-ray radiation environment. The focus of the comparative study will be the analog parameters like intrinsic voltage gain (A_V) and Early voltage (V_{EA}).

Device Characteristics and X-ray Procedure

The used MuGFETs present a fin height (H_{FIN}) and buried oxide thickness of 65 nm and 145 nm, respectively. The gate dielectric stack consists of 1 nm SiO_2 covered by 2.3 nm HfSiON, resulting in an equivalent oxide thickness of 1.5 nm and the gate electrode is composed by 5 nm TiN followed by 100 nm polysilicon. More details are found in (5). The analyzed fin widths (W_{FIN}) and channel lengths (L) are between 120 nm and 870 nm and 150 nm to 900 nm, respectively. The devices were implemented on a strained-SOI (sSOI) substrate, which is biaxially tensile stressed, and also have uniaxial stress obtained by the dual Contact Etch Stop Layer (CESL) technique. Then two different splits were analyzed:

a) tensile biaxial stress plus tensile uniaxial stress (sSOI+tCESL);
b) tensile biaxial stress plus compressive uniaxial stress (sSOI+cCESL).

The Diffractometer XRD-7000 from Shimadzu was used to irradiate the devices with an X-ray radiation effective energy of 10 krad, with an exposure rate of 20 krad(Si)/s to produce a total ionizing dose (TID) in the 1 Mrad to 50 Mrad range. Keithley 4200 Semiconductor Characterization System (Model 4200-SCS) was used to perform the device electrical characterization. The X-ray radiation is capable to produce similar TID effects in MOSFETs than those observed by proton radiation (6).

Experimental Results and Discussion

Figure 1 presents A_V ($A_V = V_{EA}.gm/I_{DS}$, where gm is the saturation transconductance, I_{DS} is the drain current and V_{EA} is the Early voltage) as a function of radiation dose for nMuGFETs with different stress conditions for L equal to 150 nm and different W_{FIN} (120, 370 and 870 nm).

Analyzing Fig. 1, it can be observed that when W_{FIN} increases, the A_V reduces, due to the worst coupling between gates and channel, that results in a device performance reduction. Besides that, A_V for nMuGFETs with tensile stress is always higher than for devices with compressive stress, due to the higher V_{EA}. Furthermore, nMuGFETs with both stresses are practically not affected by the X-ray radiation for wider W_{FIN} and L=150nm, the short-channel effects (SCE) prevails over the X-ray radiation (up to 50 Mrad). Fixing W_{FIN} at 870 nm and varying L (Figure 2), it can be seen that when the channel length increases, A_V is higher due to the V_{EA} improvement as shown in figure 3.

Figure 2 also shows that for tensile stressed devices A_V is always higher than for compressive ones due to the higher V_{EA} as shown in figure 3. For L higher than 150 nm, where SCE is not the predominant effect, the X-ray radiation reduces the A_V for both stress types, due to the generation of positive charges in the buried oxides and at the SiO_2/silicon interface. However, when A_V is compared under radiation, nMuGFETs with compressive stress show to be more affected by the X-ray radiation than devices with tensile stress. The maximum A_V variation for compressive devices is 25% for L = 600 nm and 48% for L = 900 nm, while for tensile transistors it is 18% for L = 600 nm and 42% for L = 900 nm. The higher susceptibility of the devices with compressive stress to the X-ray radiation can be explained by the higher number of defects found in the (sSOI+cCESL = tensile + compressive) nMuGFETs when compared to (sSOI+tCESL = tensile + tensile) nMuGFETs.

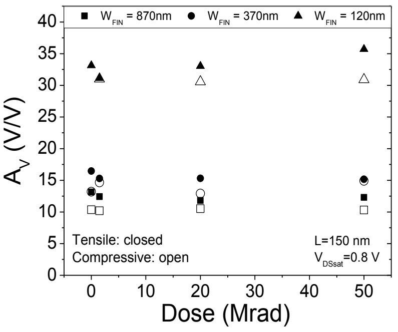

Figure 1 – Intrinsic voltage gain as a function of the radiation dose for nMuGFETs with both stress types, for different W_{FIN}.

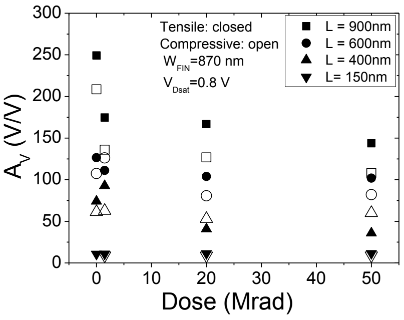

Figure 2 – Intrinsic voltage gain as a function of the radiation dose for both stress types, for different channel lengths.

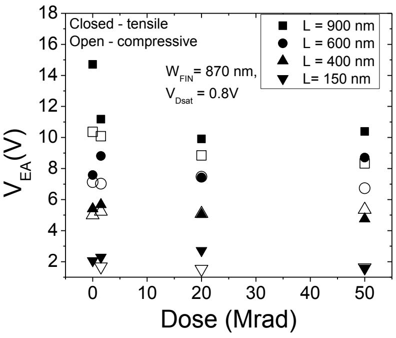

Figure 3 – Early voltage as a function of the radiation dose for nMuGFETs with both stress types, for different channel lengths.

Conclusion

Experimental results demonstrate that V_{EA} and consequently A_V with tensile stress present higher X-ray radiation robustness than those observed with compressive stress, regarding devices without SCE. The possible explanation is the higher defect densities of compressive devices built on tensile wafers, which contribute to the analog parameters degradation.

References

1. J. P. Colinge, Silicon-on-Insulator Tech.: Mat.VLSI, Kluwer, 2004.
2. V. Ferlet-Cavrois et al., IEEE Trans. Nucl. Sci., 45, 2458–2466, (1998).
3. J. P. Colinge, FinFETs and Other Multi-Gates, Springer Verlag, 2007.
4. C. Claeys et al., Solid-State Electronics, 52, 1115–1126, (2008).
5. N. Collaert et al., VLSI Symp., Dig. Technical Papers, 52–53, (2006).
6. J. Liu et al., Microelectronics Reliability 50(1), 45 (2010).
7. P. G. D. Agopian et al., IEEE Trans. Nucl. Sci., 59,707-713, (2012).