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Dopant-free CMOS on SOI: Multi-Gate Si-Nanowire Transistors for Logic and Memory Applications

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I. Introduction

In CMOS technology, NMOS- and PMOS-FETs are hardware defined by choosing the appropriate doping of the source (S) and drain (D) junctions with respect to the substrate [1]. However, in this work we report on a novel CMOS multi-gate (MG) nanowire field-effect transistor (NWFET) architecture on silicon-on-insulator (SOI) material which is free of doping. The fabricated MG-NWFETs (Fig. 1) are originally unipolar nanowire devices with midgap Schottky-barriers for S/D contacts. A tri-gate structure serves as front-gate for current control across the NWFET whereas the back-gate is used to select the desired device type (i.e. NMOS or PMOS) via field-induced accumulation of electrons or holes, respectively (Fig. 1, bottom).

II. Fabrication

Top-views and cross-sections of the device structure are shown in Fig. 1. The devices are fabricated on ultrathin-body SOI substrates from SOITEC with a top-silicon thickness of 60nm and 145nm buried oxide. A 90nm wide silicon-wire is patterned by electron beam lithography followed by RIE. A gate oxide of 12nm is formed by RTO, subsequently metallization of the S/D contacts and gate electrode is realized evaporating 70nm nickel with 180nm aluminum capping on top. S/D contacts are salicided at 500°C for 5 minutes in forming gas ambient. During annealing the mid-gap NiSi-Schottky contact [1] to the silicon nanowire is formed. In order to separate back-gates for different devices, circuits are built out of individual dies and wire bonded.

III. Results and discussion

A CMOS inverter represents the simplest form of a logic gate where significant power consumption only occurs during switching transition, when PMOS and NMOS devices are still partially turned on [2]. Using our dopant-free MG-NWFET technology, we have realized such a CMOS inverter circuit as shown in Fig. 2. By applying a back-gate voltage of -20V to the NWFET (NW1) the PMOS is defined and using a back-gate bias of +18V the NMOS NWFET (ND2) is defined. The measured inverter transfer characteristic confirms the functionality of the proposed dopant-free NWFET device architecture for CMOS logic applications. The current peak at the transition point indicates that the circuit is in fact a true CMOS inverter and not a resistive load inverter. Furthermore, by changing back-gate and supply voltage polarities, NMOS and PMOS devices are interchanged but the same transfer characteristics can be obtained. More complex circuits can be realized when using MultiSOI substrates in which the additional buried silicon layer serves as individual back-gate for each NWFET after being patterned and etched.

Charge injection and trapping in the back-gate oxide (BG-OX) can be utilized to open the possibility to create non-volatile memory devices with the same NWFET structure. After charge injection via Fowler-Nordheim tunneling (write cycle), the trapped charge in the buried oxide is causing a shift in the sub-threshold characteristics of the NWFET, as shown in Fig. 3. For a given reading voltage, the difference in the current ratios (~ 10^4) can be used to assign the stored logical "0" or "1" levels. Note, that high back-gate voltage issues can be omitted by the use of ultra-thin buried oxide layers (e.g. 10nm vs. 145nm).

In conclusion, the ability to select the device type simply by applying an appropriate back-gate bias provides additional flexibility in reconfigurable logic design (e.g. FPGA) as well as system-on-chip (SoC) applications. Furthermore, non-volatile memory function can be easily implemented in the dopant-free MG-NWFET architecture by means of buried oxide charge injection and trapping.

References

[1] E. Bucher et.al., *Appl. Phys. A* **40**, pp. 71-77 (1986)

[2] F. Wanlass and C. Sah, International Solid State Circuits Conference Digest of Technical Papers, pp. 32-33 (1963)

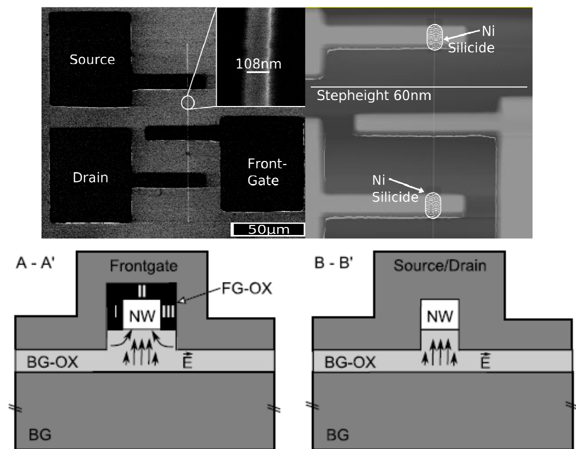

Fig. 1: SEM (top left) and AFM (top right) images of the fabricated NWFET device structures. Cross-sectional drawings of the front-gate (bottom left) and S/D (bottom right) regions to illustrate multi-gate field-effect.

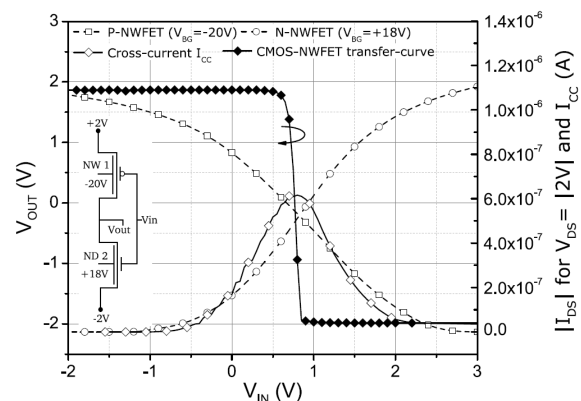

Fig. 2: Measured transfer characteristics of dopant-free CMOS-NWFET inverter. The current peak indicates that it is a true CMOS inverter circuit. By changing back-gate and supply voltage polarities, NMOS and PMOS devices are interchanged but the same transfer characteristics can be obtained (not shown here).

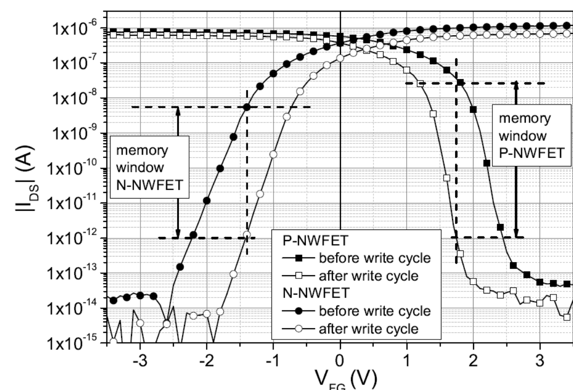

Fig. 3: Measured memory effect in a dopant-free CMOS-NWFET for both, PMOS and NMOS operation (i.e. sub-threshold curves).