Strain-enhanced performance of Si-Nanowire FETs

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Multigate (MG) transistors are strongly attractive for future CMOS technology nodes, as these architectures present good immunity to short channel effects through a better electrostatic control [1,2]. Several demonstrations of MG-FETs have already been reported, including Gate-all around (GAA), FinFET, Trigate and omega-gate transistors (see for example [2] and refs. therein). The optimization of these advanced devices is not trivial since conduction occurs in inversion surfaces with multiple crystallographic orientations.

Stress engineering, widely used for high-performance logic applications, can drastically improve the electrical performance of MOSFETs by increasing the carrier mobility [3]. The combination of a MG architecture with stress, if well understood, can lead to a further increase of the drive current together with better electrostatic integrity. The strain effect in these "non-planar" devices still needs theoretical as well as experimental investigations [4].

In this work we present a study on the effect of strain in Si NanoWire (NW) TriGate (TG) and Ω-Gate (ΩG) transistors. We present our results on the electrical characterization of these advanced devices, with special attention to the carrier mobility, as transport properties mainly drive the electrical performance.

The Si NW devices have been fabricated using top-down approach by optical lithography followed by resist trimming process [5]. The NWs MOSFETs were fabricated on (110) oriented unstrained- or strained- SOI wafers, with ~10nm silicon thickness (Fig.1). Ω-Gate was formed with additional H_2 annealing. Strained NWs are obtained from sSOI substrate: the initial ~1.4GPa biaxial tensile stress reduces to a uniaxial tensile stress due to lateral relaxation (Fig.1b). All channels are oriented along [110] direction. Devices with different widths from wide (W_{top}=10µm) to narrow (NW with W_{top} down to 10nm) geometry have been measured.

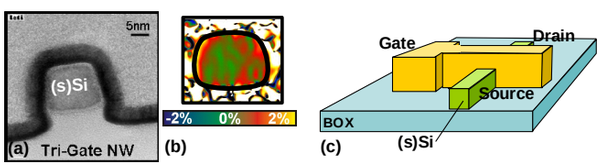

Figure 1: (a) Cross-sectional TEM image of a TriGate Si-NW transistor. (b) Strain mapping calculated from high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) image of sSOI NW transistor (the color mapping corresponds to the lattice mismatch with respect to unstrained silicon [9]). (c) Schematic of the Si NW transistors fabricated from (s)SOI substrate.

Transport properties of (s)Si NW transistors have been studied through mobility measurement on long channel N- and P-MOSFETs [5-8]. We have shown that conduction in strong inversion can mainly be described by the independent contribution of the (100) top-surface and the (110)-sidewall surface for TG-NWs. The addition of a uniaxial tensile strain is very effective in both TG and ΩG devices. In particular we have thus obtained electron mobility enhancement in NMOS sSi-NWs (Fig2a), which overcomes the electron mobility loss inherent to unstrained Si-NWs with (110)-sidewalls. Low temperature measurements down to 20K have also been performed. Thanks to these measurements, we have evaluated and discussed the contribution of the different scattering mechanisms involved in transport in unstrained and strained NWs.

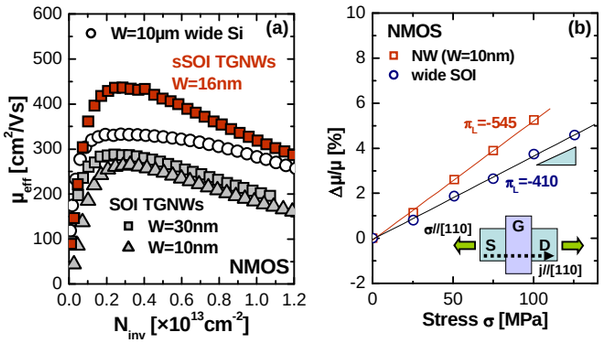

Figure 2: (a) Effective electron mobility μ_{eff} measured as a function of inversion carrier density N_{inv} for SOI and sSOI TG-NW FETs, compared with a *conventional* wide SOI device. (b) Measurement of the longitudinal piezoresistance coefficient π_L for a NMOS TG-NW and a wide SOI FET, showing the mobility enhancement expected from an additional uniaxial tensile stress (units of π_L: $10^{-12}Pa^{-1}$).

Finally the strain effect on transport properties have been more deeply investigated through extraction of the piezoresistive (PR) coefficients [10,11]. This characterization technique evaluates the mobility change $\Delta\mu/\mu$ due to a uniaxial stress, applied by a wafer bending apparatus (Fig.2b). The obtained set of PR coefficients (longitudinal π_L and transversal π_T) provides an additional insight on the potentiality of strain in complex architecture like Si TG- or ΩG NWs, which will be further discussed.

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