Integration and Characterization of Graphene-Insulator-Graphene Junctions

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There recently has been significant interest in electron devices consisting of a graphene-insulator-graphene (GIG) junction. For example, the graphene bilayer pseudospin field-effect-transistor (BISFET) is based on the condensation of excitons formed between the two graphene layers resulting in negative differential resistance at very low interlayer voltage (1-3). GIG devices can also be operated in a single particle tunneling mode resulting in either negative differential resistance (4) or a very steep subthreshold swing (5,6). There are numerous materials and characterization challenges for these devices. For example, high quality large area single layer graphene will be necessary, high quality interlayer dielectrics are required which do not dramatically perturb the graphene, and techniques to characterize the relative orientation of the graphene sheets will be required.

We have recently developed a variety of designs for bilayer devices consisting of large area 2D-to-2D graphene. Our fabrication process involves transfer of monolayer graphene onto an oxide/Si substrate, metal contact deposition on bottom graphene layer, deposition of a dielectric, transfer of top graphene monolayer, contact deposition on the top graphene layer, and formation of top gate stack. As a first step to graphene tunnel transistors, we have attempted to demonstrate low subthreshold swing using various tunnel dielectrics. The back-gate dielectric was also varied to keep the equivalent oxide thickness and the off-state current low. Figure 1 shows a typical device with an atomic layer deposited TiO_x/Al_2O_3 tunnel dielectric stack exhibiting a subthreshold swing of < 100 mV/decade.

In this talk, a variety of issues related to integration, fabrication and characterization of these structures will be described including: transfer and cleaning processes of CVD graphene, deposition of high quality dielectrics, issues related to metal contacts, and characterization of relative misorientation of the graphene sheets using Raman spectroscopy.

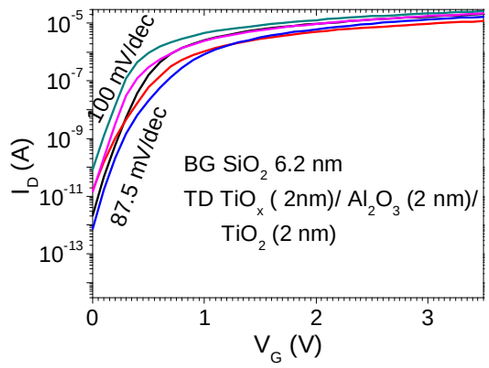

Fig. 1. (a) Tunnel current vs. back gate voltage for a typical GIG tunnel transistor. V_D = 0.02 V.

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