Influence of 45° Substrate Rotation on the Analog Performance of Biaxially Strained Silicon SOI MuGFETs

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The Multiple Gate devices (MuGFET) are nowadays one of the most important contenders for the sub-22 nm MOSFET generation due to excellent control of the gate on the channel (1). Additionally to the better control provided by tri-gate, the use of controlled mechanical stress is largely used in the semiconductor industry for boosting the carrier mobility in the channel. Biaxial strain is more effective for longer and wider devices due to the relaxation of the stress along both directions of the channel. This relaxation is observed in approximately 100 nm from the edges (2). In a narrow fin, the predominance of the drain current flows vertically in the sidewalls, that is in the (110) orientation, and only a small portion of the current flows in the (100) plane (3). The problem associated with the electron mobility is due to a degradation in the (110) crystal orientation with respect to (100) whereas the mobility of holes is improved (4). By rotating the substrate 45° all the conduction planes will be (100) (5) and the improvements of substrate rotation on device performance have been discussed in the literature (6). This works proposes for the first time an analysis of the influence of 45° substrate rotation on the biaxial stress impact on basic parameters and analog perspective for several channel widths. The strained 45° rotated and non-rotated strained nMuGFETs evaluated in this work were fabricated in Imec following the process described in (7). The 45° rotated strained and non-rotated strained nMuGFETs were fabricated in SOI wafers with 1.5 GPa intrinsic biaxial tensile strain. The buried oxide is 145 nm, and the top silicon layer thickness is 60 nm. The gate stack is formed by a 1 nm SiO_2 followed by 2.3 nm HfSiON, resulting in an equivalent oxide thickness (*EOT*) around 1.7 nm for strained and 45° rotated strained nMuGFETs. No channel doping or halo implantation is applied during the processing, keeping the p-type doping level in the order of 10^{15} cm^{-3}. The measured devices have 5 parallel fins per transistor and a channel length (L) of 1μm.

The curves of drain current (I_D) as a function of gate voltage (V_{GS}) were obtained for a drain voltage (V_{DS}) of 50 mV for all studied devices. From these curves the maximum transconductance ($g_{m,max}$) as a function of W_{fin} has been extracted (Fig. 1 left axis). In Fig. 1 one can see an $g_{m,max}$ improvement (hence carrier mobility) with W_{fin} increase, independent of substrate rotation. In case of strained rotated devices, the $g_{m,max}$ improvement is reduced in comparison to strained devices without substrate rotation. Analyzing the reduction of $g_{m,max}$, we extracted in Fig. 1 at the right axis the percentage difference between strained over rotated strained to quantify the reduction of $g_{m,max}$ in strained rotated devices. From Fig. 1 (right axis) a reduction is found of 13 % and 45 % for W_{fin} = 870 nm and 20 nm, respectively. The reduction in the strain due to rotation of the substrate is in accordance with the ref (8) where a reduction of 50 % in transconductance gain is provided by mechanical stress in the (100) orientation for a narrow fin (20 nm). Another important observation is given by ref. (9) using Monte Carlo simulations of bulk FinFETs, associating the increase of carrier mobility with the reduction of electron effective mass, being more evident for the (110) orientation. These explanations are in accordance with the measured results as for wide fins the effect of biaxial mechanical stress is evidenced as well as for both non-rotated and rotated devices the predominance of carrier mobility is in the top surface (100) plane, reducing the effect of substrate rotation and consequently minimizing the difference of $g_{m,max}$ for rotated over non-rotated devices. By narrowing W_{fin} a reduction of biaxial strain effectiveness occurs for both devices due to stress relaxation. However, for rotated devices all conduction planes are in the (100) orientation making the reduction of effective mechanical stress more evident, causing a higher difference between non-rotated and rotated devices in maximum transconductance.

The analog parameters where extracted at V_{DS} = 0.85 V and V_{GT} = 0.2 V. In Fig. 2 one can see an extracted output conductance (g_d) as a function of W_{fin}. The g_d shows a degradation as W_{fin} increases independent of substrate rotation which is related to the better coupling between the gates improving the output conductance. The strained non-rotated and rotated devices present practically the same values of g_d for all W_{fin}, resulting in marginal influence of g_d caused by substrate rotation. Also in Fig.2 the g_m is presented and shows an increase for both strained devices for any W_{fin}, being more evident for non-rotated strained devices. Combining the g_m and g_d the intrinsic voltage gain (A_V=g_m/g_d) has been calculated as a function of W_{fin} (Fig.3). The results show a reduction of A_V with W_{fin} reduction for all devices. In addition, a larger A_V was found for strained non-rotated devices for all W_{fin} in comparison to rotated devices. In this case for rotated strained devices the g_m improvement is reduced by substrate rotation but the g_d degradation remains close to non-rotated strained devices and consequently a higher reduction of A_V for rotated strained devices was found.

Acknowledgments

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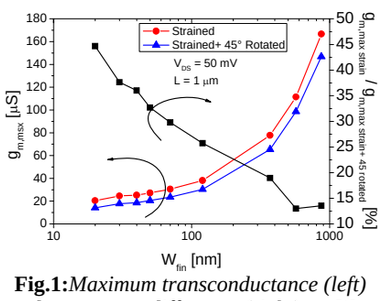

Fig.1: *Maximum transconductance (left) and percentage difference (right) vs. W_{fin}.*

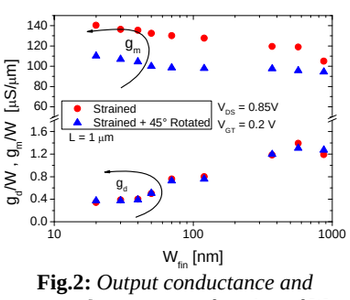

Fig.2: *Output conductance and transconductance as a function of W_{fin}.*

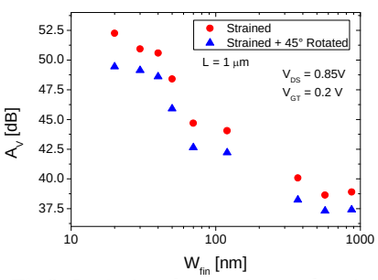

Fig.3: *Intrinsic voltage gain as a function of W_{fin}.*