Identification of Deep Levels Associated with Extended and Point Defects in GeSn Epitaxial Layers using DLTS

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Alternative channel materials, such as Ge for p-MOS and III-V for n-MOS, owing to their high intrinsic carrier mobilities, are increasingly being studied as candidates for below 14nm CMOS technology node. A further performance improvement of these compound transistors can be achieved by mobility enhancement via strain engineering. The recent developments, in hetero-epitaxial growth of strained GeSn channels, deposited on relaxed Ge template, exemplify the hole mobility boost from the resulting in-plane biaxial compressive stress [1,2].

While the epitaxial growth of these high mobility channel materials on Si allows relative low cost integration of the technology in Si CMOS process line, it also makes the active device regions prone to threading dislocations (TDs) and other crystal defects owing to lattice mismatch with Si. The TDs and bulk crystal defects are known to introduce defect levels in the band gap of the semiconductors, which can act as traps or generation/recombination centers, which affect the mobility and noise properties of the semiconductor, prominently leading to enhanced leakage current. Another important issue to be addressed is the interface quality between semiconductor and high-k dielectric deposited on them, which influences surface potential, charge transport and frequency response of the devices [3]. Therefore, it is viable to say that the key to success of compound CMOS device technology lies in control and understanding of the defects in both, the active region and the oxide-semiconductor interface.

Here, the interface and bulk defect states are studied in unintentionally doped compound p-type $Ge_{0.93}Sn_{0.07}$/Ge layers grown on p-Si at 320°C using atmospheric pressure chemical vapor deposition (AP-CVD) [4]. A $(GeSn)O_2$ or GeO_2 interlayer was formed and 9nm Al_2O_3 was deposited by MBE. MOS capacitors of variable diameters were fabricated by depositing Ni contacts by thermal evaporation [5]. A well established technique, deep level transient spectroscopy (DLTS) is used for the study, which allows measurement of low density of defect states ($N_t \approx 10^{-5} N_D$) [6]. Capacitors are biased in depletion and accumulation, to identify the bulk and interface traps respectively. The trap concentrations(N_t), capture cross-sections (σ) and positions of trap levels in the band gap (E_a) are calculated. More interestingly, complementary frequency-scan DLTS is performed at fixed temperature to study trap kinetics and identify the origin of defect states [7–9].

Figure 1, shows the filling pulse isothermal measurements carried out on a 300um diameter capacitor at temperatures corresponding to activation energies of the trap levels. The Fourier b_1 component of the transient is proportional to the concentration of filled traps, while abscissa is the duration of the filling pulse. Since separation between active defect sites in a dislocation line is on atomic scale, carrier trapping at one defect site in a dislocation line creates a time dependant coulombic potential barrier which hinders capture at adjacent sites. This leads to time dependent logarithmic capture kinetics for dislocation, in comparison to point defects which saturates with increasing pulse width as shown in the figure.

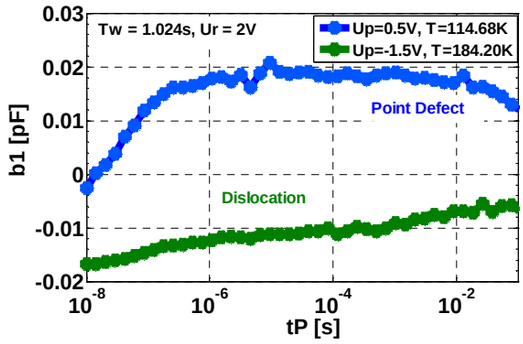

Fig1: Isothermal DLT spectra of GeSn-based 300um diameter MOS capacitors, using a period width of 1.024s, quiescent reverse bias, Ur of 2V and filling pulse amplitude, Up of 0.5 and -1.5V for traps in bulk and interface respectively. The measurement is performed at 2 different temperatures.

In addition to identifying the defect type, a detailed analysis of the DLT spectrum is carried out. By capacitance voltage measurements, it is observed that the free carrier concentration varies with temperature. It is speculated that freeze out of carriers occurs at lower temperatures in deep acceptor states. It will also be illustrated, that the traps associated with dislocations, ($\sigma = 1.57 \times 10^{-15} cm^{-2}$, $E_a \approx E_V + 0.262\, eV$) exhibit field dependent emission. Furthermore, the studied DLT spectrum also shows the presence of defect states due to tunneling in the gate oxide [10,11].

In summary, DLTS of MOS capacitors on GeSn/Ge epitaxial layers indicates the presence of point defects and threading dislocations in bulk Ge. In addition, slow oxide traps at the interface of high-K dielectric and $Ge_{0.93}Sn_{0.07}$ layer have been detected.

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