Temperature Effects on Silicon Nanocrystal Memories

V. Della Marca[*+£], J. Amouroux[*+£], G. Molas[£],
J. Postel-Pellerin[+], F. Lalande[+], P. Boivin[*], J-L. Ogier[*]

[*]STMicroelectronics, 13106 Rousset, France
[+]Im2np-CNRS, Université Aix-Marseille, 13451 Marseille, France
[£]CEA-LETI, MINATEC, 38054 Grenoble, France

The microelectronic industry requires more and more low consumption and high reliability solutions. In this scenario the silicon nanocrystal memories (Si-nc) are one of the most mature technologies able to replace the Flash floating gate in NOR embedded applications. The main advantages of Si-nc memories are: the full compatibility with the CMOS process with a reduced number of masks [1] and the robustness against SILC [2]. In this paper we present an experimental work on the optimized silicon nanocrystal cell industrially manufactured, where the reliability and the energy consumption are improved [3]. In particular the impact of temperature on cell programming window is shown. Moreover programming by channel hot electron (CHE) and erasing by Fowler-Nordheim (FN), we demonstrated for the first time at our knowledge that it is possible to achieve 1Mcycles endurance characteristic in the temperature range of [-40°C; 150°C].

The silicon nanocrystals are grown by Low Pressure Chemical Vapor Deposition (LPCVD) on the tunnel oxide top surface with a two-step process [4]. Using this approach the density and diameter (Φ) of Si-nc can be independently controlled. The nanocrystals are observed in top view using the Critical Dimension Scanning Electron Microscopy CDSEM [5]; their average size and density are extracted with a technique of image processing (Fig. 1). Two types of samples were compared with different nanocrystals diameters (Φ~9nm and Φ~12nm) in order to show the improvements due to the coupling factor increasing. The Si-ncs were deposited on 4.2nm tunnel oxide.

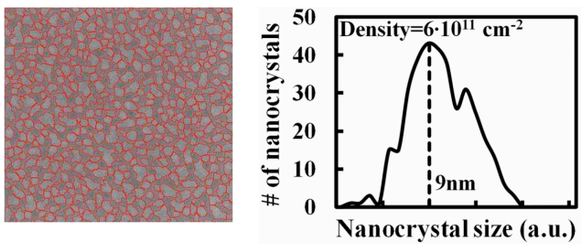

Fig.1 Silicon nanocrystal top view using Critical Dimension Scanning Electron Microscopy (CDSEM), and nanocrystal diameter extrapolated distribution.

In Fig. 2a we show the impact of temperature during the channel hot electron programming operation on the sample with 12nm nanocrystals. The threshold voltage (Vt) evolution is obtained using a drain voltage (Vd) of 4.2V and applying the 1.5V/µs ramp between 3V and 9V on gate terminal (Vg). The programming window decreases increasing the temperature because the current in the channel decreases as well as the injection probability [6]. In Fig. 2b the FN erase kinetic characteristics are obtained applying a 5kV/s ramp on gate terminal from -14V up to -20V. In this case, the erase efficiency increases with the temperature. This is justified assuming that the dominant conduction mechanism is traps assisted [7].

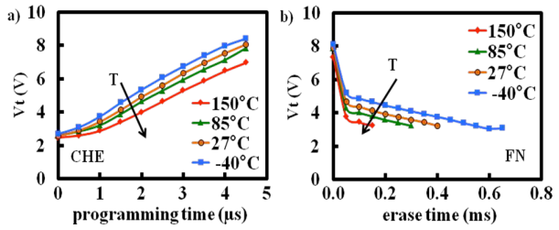

Fig. 2. Temperature dependence of a) channel hot electron programming and b) Fowler-Nordheim erase.

The impact of the covering ratio on the endurance is also investigated. Fig. 3 presents the endurance results for the Si-nc cell at 27°C. The cells are programmed by CHE (Vg=9V, Vd=4.2V, tp=1µs) and erased by FN operation (Vg=-18V, 5V/ms ramp followed by 1ms plateau). Increasing the covered area the erase operation is improved. The sample, with the higher covering ratio, shows a programming window of 5.5V for the virgin state and of 4V after 1Mcycles.

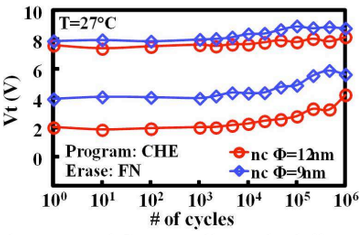

Fig. 3. Endurance of Si-nc cells with different covering ratios. CHE programming and FN erase. T=27°C.

Using the same program/erase conditions we repeated the experiment varying the temperature (T=-40°C and T=150°C). In Fig. 4 the results are shown for the Si-nc cell with the higher covering ratio (Φ=12nm). The programming window after 1Mcyles remains bigger than 4V independently on the temperature. One can notice that increasing the temperature the characteristic shifts toward the lower voltages.

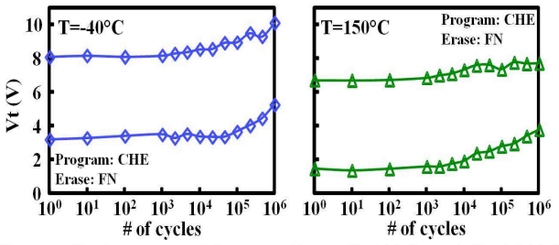

Fig. 4. Endurance of Si-nc cells at T-40°C and T=150°C. CHE programming and FN erase.

In conclusion this experimental study shows the temperature effects on the silicon nanocrystal memory cell. We characterized the channel hot electron programming and Fowler-Nordheim erase kinetics in a temperature range from -40°C to 150°C. Moreover the impact of nanocrystals size on programming window and endurance is studied. Finally we demonstrated for the first time the cell functionality in a wide temperature range up to 1M program/erase cycles maintaining the programming window larger than 4V.

[1] B. De Salvo, et al., Tech. Dig. of IEDM, pp. 597-600, 2003.
[2] C.M. Compagnoni, et al., Proc. IRPS, pp. 506-512, 2003.
[3] V. Della Marca, et al., Proc. CAS, vol 1, pp. 103-106, 2012.
[4] F. Mazen, et al., Proc. MNE, vol. 73-74, 2004.
[5] J. Amouroux, et al., Proc. MRS, vol 1337, 2011.
[6] B. Eitan, et al.,Trans. Elec. Dev., vol.28, no. 3, pp. 328-340, 1981.
[7] M.A.Rafiq, et al., JAP, vol. 104, pp. 123710. 2008.