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InP-Si BiCMOS Heterointegration using a Substrate Transfer Process

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In this work, transmitters for broadband radio links are addressed in the frequency range 100...500 GHz, which are key building blocks for future wireless communication systems. What makes this work unique is that these components are to be realized by means of an InP-on-BiCMOS wafer-level process technology. In contrast to other attempts, the technology demonstrated here is based on preprocessed BiCMOS and transfer substrate (TS) InP HBT technologies, respectively. This allows to combine the favorable power performance of III-V circuits with the advantages of BiCMOS circuits such as complexity and integration density, without critical performance trade-offs of the individual technologies. Critical problems in such a technology are RF interconnects. DC- and RF-interconnects between the InP and BiCMOS circuits have been tested, showing the feasibility of the wafer-level bond process for heterointegration of TS InP and BiCMOS. For that purpose a 4-metal Al back-end was built on the silicon wafer with silicon dioxide as interlayer dielectric. After the wafer bond process the TS InP with 3-metal Au in benzocyclobutene (BCB) as interlayer dielectric has been realized in top of the processed BiCMOS to test the best transmission line configuration. The BiCMOS backend needed some adaptation for the wafer-bond process in terms of planarization of the passivation. The standard process uses a SiO_2- and a SiN-layer as passivation stack. For the planarization of the top-metal 2 level (TM2 in Fig.1, 3µm Al thickness) a thick SiO_2 was deposited by HDP and PECVD. It was planarized by chemical mechanical polishing (CMP) and finally etched back until the Top-Metal 2 pads reach the surface. The TS InP HBT process has been adapted to contact this top surface. A backside polish process was developed to enable backside lithography. The backside lithography allows to produce bond alignment marks with a front to back side misalignment smaller than 300 nm. After that the 200 mm wafers were cut into four 3” wafers to enable the bond process with the 3” preprocessed InP wafers with subsequent removal of the unused InP by wet chemical etching. The wafer bond process and the electrical measurements at the finished wafers were carried out at the FBH. We demonstrate the feasibility of InP HBT / Si BiCMOS integration with a wafer bonding accuracy < 10 µm resulting in low DC contact resistance of about 1 Ohm. RF measurements (Fig. 2) demonstrated low insertion loss of the BiCMOS-InP via transitions (G2-TM2) compared with a reference line (GD-G2) completely in BCB, and the simulated losses.

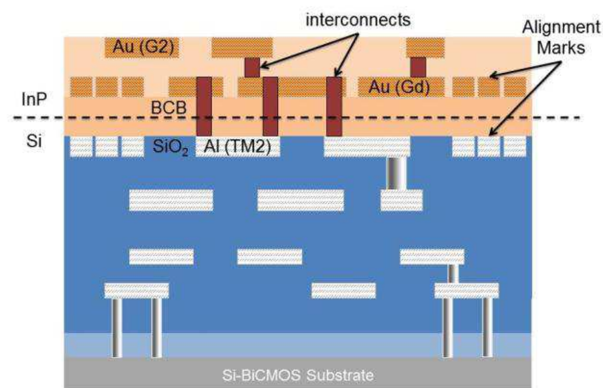

Fig. 1: Scheme of the back-end for InP-Si integration

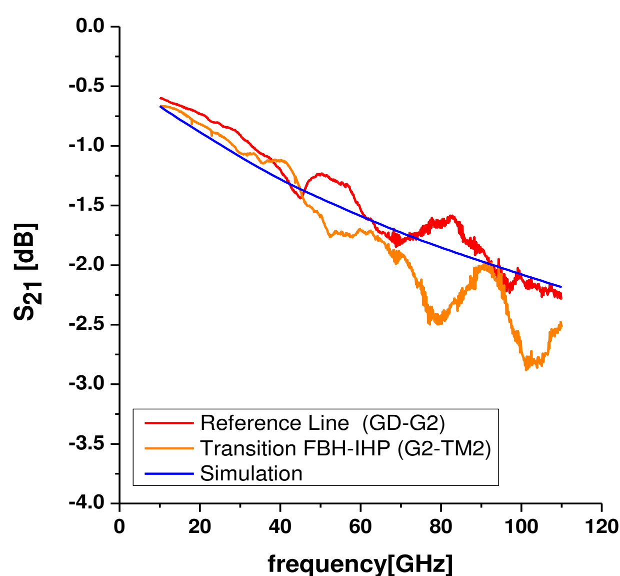

Fig. 2: Low insertion loss of the RF-BiCMOS-InP via transitions consisting of a microstrip and a special designed vertical interconnect area landing on a small TM2-Al Pad for reduction of the parasitic capacitance.