

Semiconductor Film Bandgap Influence on Retention Time of UTBOX SOI 1T-FBRAM

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The 1T-FBRAM (single transistor floating body RAM) using the BJT (Bipolar Junction Transistor) effect to write '1' has been reported as the best way to reach longer retention times and higher sense margins (1). Nevertheless, to achieve the 64 ms specification for standalone DRAM (2), its retention time still needs to be further improved.

Motivated by the Si-Ge and SiC alloys that have been studied for optoelectronics and memory applications (3-7), this work analyzes the semiconductor film bandgap (E_g) influence (figure 1) on Ultra-Thin-Buried-Oxide Semiconductor-On-Insulator (UTBOX SOI) 1T-FBRAM performance in order to achieve longer retention times.

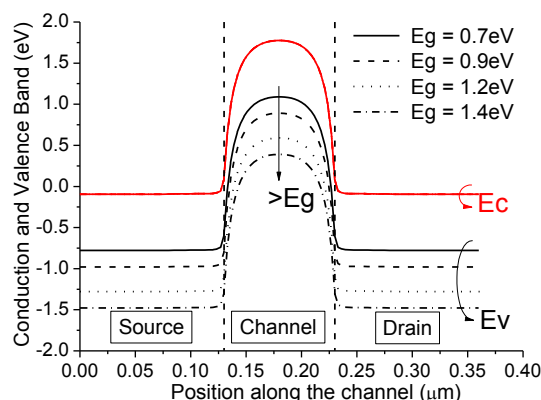


Figure 1: Different semiconductor bandgaps on Semiconductor-On-Insulator nMOSFET.

The UTBOX SOI structure simulated in this work was based on the process information of reference (8). The gate oxide thickness is 5 nm of SiO_2 and the buried oxide thickness (t_{BOX}) is 10 nm. The gate electrode is TiN. The channel doping level (N_A) is $1 \times 10^{15} \text{ cm}^{-3}$ and its dimensions ($L \times W \times t_{\text{SI}}$) are equal to 100 nm, 1 μm and 20 nm, respectively. Below the buried oxide there is a ground plane, which is used as a back gate.

The results were obtained through numerical simulations using the Kane's model for band-to-band-tunnelling (BTBT) and the Poole-Frenkel Barrier Lowering for Coulombic wells as the traps model (9) while applying the biasing scheme as shown in figure 2.

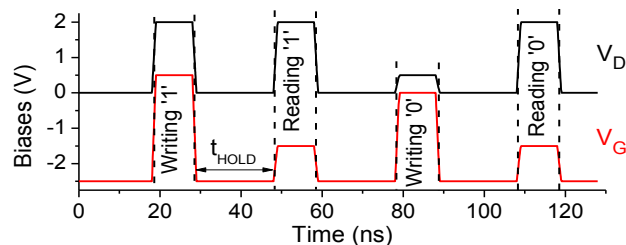


Figure 2: Biasing scheme of the FBRAM cell.

Figure 3 shows the currents read at states '1' and '0', I_1 and I_0 , respectively, as a function of hold time (t_{HOLD}) and figure 4, the extracted retention time as a function of the bandgap.

The main and most significant advantage obtained in increasing the channel bandgap is the longer retention time (defined as the maximum time between a write and a read,

in which the bit is still read correctly) as can be seen in figures 3 and 4.

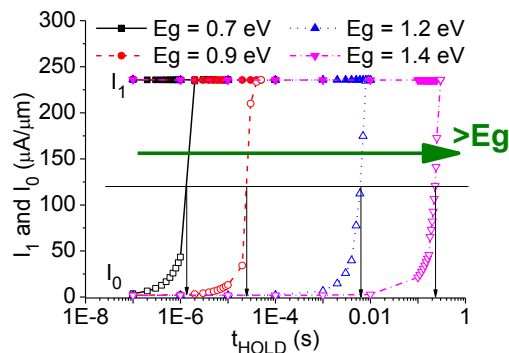


Figure 3: I_1 and I_0 as a function of hold time for different bandgaps.

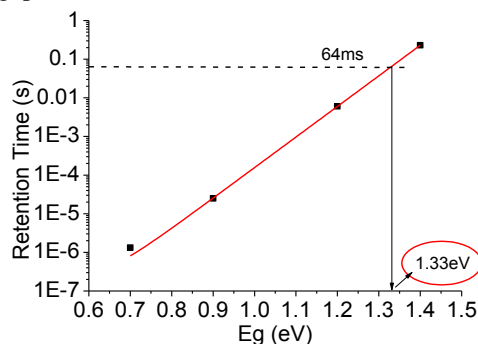


Figure 4: Extracted retention time for different bandgaps.

From figure 3, a time shift for '0' degradation is observed when the bandgap is increased from 0.7 eV to 1.4 eV, resulting in an improvement of 5 orders of magnitude (figure 4) on retention time. This can be related to the lower generation rate expected for higher bandgaps. According to this curve, the bandgap has to be higher than 1.33 eV for achieving a better retention time than standard DRAM.

Figure 5 shows that a lower generation rate along the channel is observed for a higher bandgap, confirming the reason for lower '0' degradation and, thus, the longer retention time.

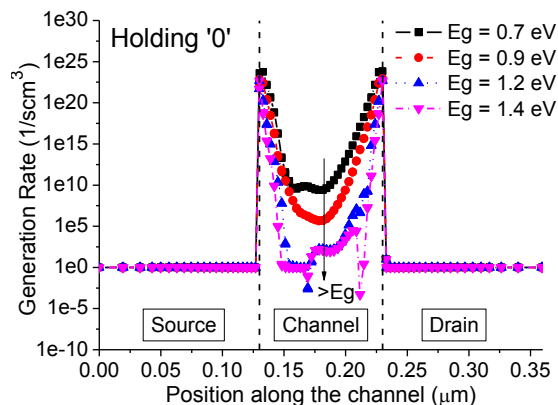


Figure 5: Generation rate along the channel during holding '0' at 1 nm below the front interface for different bandgaps.

References

1. S. Okhonin et al., IEDM Tech., 137, 925 (2007).
2. ITRS, ed. 2011, <http://www.itrs.net>
3. R. A. Soref, Proc. of IEEE, 81, 1687 (1993)
4. F. Giorgis et al., Journal of Non-Crystalline Solids, 227, 465 (1998)
5. P. Tang, R. Huang, D. Wu, Jpn. J. Appl. Phys., 49 (2010), 04DD02
6. J.-W. Han et al., IEEE Elec. Dev. Lett., 32, 850 (2011)
7. S.-W. Ryu et al., Proc. of IEDM, 1 (2008)
8. N. Collaert et al., IEEE Int. SOI Conference, 1 (2009).
9. ATLAS Device Simulation, User's Manual, version 5.14.0.R, Silvaco International, Santa Clara, 2010.