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On the optimization of ebeam lithography using Hydrogen SilsesQuioxane (HSQ) for innovative self-aligned CMOS process

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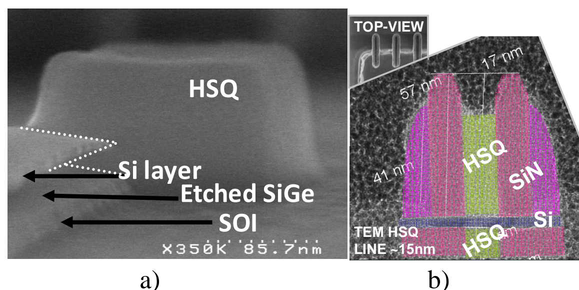
Next generation CMOS architectures tend to thin-film devices (and multi-gate devices, such as FinFET or TriGate) [1,2], and ultimately to Gate-All-Around devices thanks to their higher electrostatics integrity at short gate length compared to conventionnal planar CMOS. This paper presents recent optimizations of ebeam lithography using HSQ (Hydogen-SilsesQuioxane, $H_8Si_8O_{12}$) resist, used to form self-aligned cavities and finally gate-all-around or double-gated devices.

HSQ has demonstrated many features making it an attractive candidate for such applications: it is a high-resolution [3] and low Line-Edge-Roughness [4] negative tone inorganic resist for electron beam lithography [5] that can be converted into amorphous silicon oxide after exposition/bake treatment. It is compatible with conventional front-end silicon technology devices manufacturing and presents excellent gap/cavity fill and planarization performances. Finally, its compatibilty with EUV radiation [6] paves the way to the end of the semiconductor roadmap.



a) b)

Fig.1 – a) HSQ pattern around a Si layer.
b) 15nm HSQ line with nitride spacer.
HSQ exposition is possible through Si.

Previous works have demonstrated that HSQ can be exposed through a Si layer up to 16nm thick [7], and here of about 6nm (Fig. 1), with identical feature dimensions above and below the Si layer. Simulation also demonstrated that neither loss nor diffusion occurs for the electron-beam and the crystalline silicon layer is not modified during this process [7].

Silicon-On-Nothing integration [8] can provide, after an epitaxial step of SiGe and Si followed by selective SiGe etch, the formation of a suspended Si layer. The HSQ exposition through this Si layer can form a trench, which could subsequently be filled by gate material to create a self-aligned double-gate transistor [9] as schematized in Fig.2.

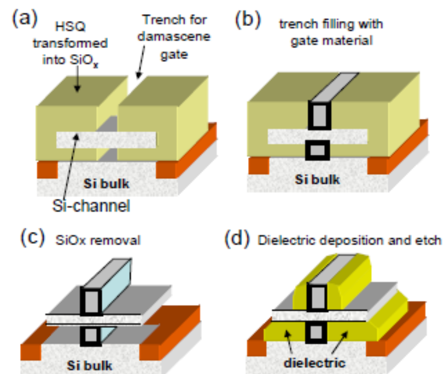


Fig.2 – HSQ-based integration steps to create a gate-first transistor with self-aligned double gates [9].

In order to form short channel devices, small HSQ trench widths have to be achieved. Despite its high-resolution performances, HSQ is also known for its low contrast which is a drastic limiting factor in such dark-field (inverted pattern) applications. In this paper we will discuss the proposed solutions to improve the lithographic step by both process and data preparation optimizations by ASELTA. In particular a multi-pass electron lithography technique [10-11] is used: simulations of dose profile with or w/o multi-pass feature demonstrate a significant change in contrast and trench dimension (Fig.3, top).

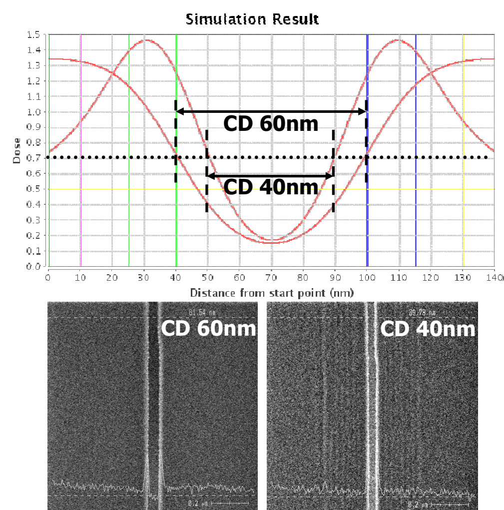


Fig.3 – Top)- Simulated dose profile in HSQ w/ and w/o electron beam multi-pass. Bottom)- HSQ trenches width reduced from 60nm down to 40nm.

The above (Fig.3) demonstrate for the first time the possibility to reduce the critical trench dimension down to 40nm by using such optimized lithographic step with a 300mm Vistec VSB 50 keV ebeam tool and a DNS RF^3 track. In this work we will also propose experiments and integration schemes to fulfill the needs for the reduction of final gate length in ultimate MOS devices.

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