Analysis of Bias-Stress-Induced Charge Trap Sites in Organic Transistors

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In this research, we investigate the bias-stress-induced charge trap sites located in polymer gate-dielectrics (PGDs) and present a novel strategy for separating out charge traps in organic semiconductors and gate-dielectrics. It is firstly demonstrated that the polymer chain-ends of PGDs can trap charges; the bias-stress stability is reduced without changes in the mobilities of the transistor devices as well as the morphologies of the organic semiconductors.[1] Under bias stress in ambient air, the drain current decay and the threshold voltage shift are found to increase as the molecular weight (MW) of PGD decreased (MW effect). (**Fig. 1**) This MW effect is caused by the variation in the density of polymer chain-ends in the PGDs with MW: the free volumes at the polymer chain-ends act as charge trap sites, resulting in drain current decay during bias stress. The free volumes at polymer chain-ends are sufficiently large to allow the residence of water molecules, the presence of which significantly increases the density of charge-trap sites.

Secondly, we present a novel strategy for analyzing bias-stress effects based on a four-parameter double stretched-exponential formula.[2] The formula is obtained by modifying a traditional single stretched-exponential expression comprising two parameters (a characteristic time and a stretched-exponential factor) that describe the bias-stress effects. The expression yields two characteristic times and two stretched-exponential factors, thereby separating out the contributions due to charge trapping events in the semiconductor layer-side of the interface and the gate-dielectric layer-side of the interface. We found that the gate-dielectric layer, in general, plays a more critical role than the semiconductor layer in the bias-stress effects, possibly due to the wider distribution of the activation energy for charge trapping. Furthermore, the presence of a self-assembled monolayer further widens the distribution of the activation energy for charge trapping in gate-dielectric layer-side of the interface and causes the channel current to decay rapidly in early stage.

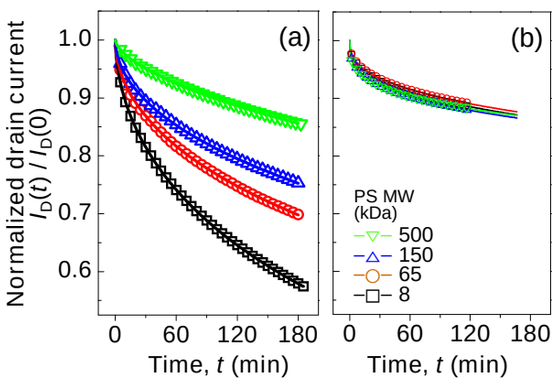

Fig. 1. Time-dependent I_D decay under constant bias-stress (V_G = -60 V, V_D = -5 V) in (a) ambient air and (b) vacuum. Open circles, experimental results; solid lines, fits to the experimental results with the stretched exponential function ($I_D(t)=I_D(0)\exp\{-(t/\tau)^{\beta}\}$).

Reference

[1] H.H.Choi, W.H.Lee, K.Cho, *Adv. Funct. Mater.*, 22, 4833 (2012)
[2] H.H.Choi, M.S.Kang, M.Kim, H.Kim, J.H.Cho, K.Cho, *Adv. Funct. Mater.*, DOI:10.1002/ adfm201201545 (2012)