Performance of Junctionless Nanowire MOSFET as a Quasi-linear Resistor

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Introduction

The operation of MOS transistors in linear region is of great interest in several analog circuits, such as in filters, where they are used as tunable resistors (1, 2). In this configuration, source and drain are used as resistor terminals and the gate voltage (V_{GF}) tunes the on-resistance (R_{ON}) to the target value. However, MOSFETs very non-linear I-V characteristics constitute an important drawback in these applications as it generates undesired harmonics to the fundamental input signal.

Junctionless nanowire transistors (JNTs) have been recently proposed and constitute a promising alternative to circumvent the technological challenges of realizing ultra-sharp doping concentration gradients in junctions for advanced CMOS technologies (3). The device is a silicon nanowire with constant heavy doping through source, channel and drain as represented in Fig. 1. JNTs have been demonstrated to provide improved characteristics for analog application in comparison to inversion-mode (IM) MuGFETs, such as reduced output conductance (4) and harmonic distortion (HD) when operating as an amplifier (5). However, no information about the operation of JNTs as quasi-linear resistor has been presented up to now. In this work, an experimental analysis of JNTs working as resistor is presented as a function of fin width (W_{fin}) and temperature (T), focusing on the on-resistance and linearity.

Results and Discussion

JNTs were fabricated on SOI wafers with 340 nm buried oxide, following the process described in (3). The silicon layer was patterned into nanowires with L=1 µm, and W_{fin} ranging between 20 nm and 40 nm with fin height (H) of 10 nm. The doping concentration is to about 5×10^{19} cm^{-3} and the gate stack is formed by 10 nm-thick gate oxide and 50 nm-thick P+ polycrystalline silicon. Fig. 2 presents the quasi-linear measured I_{DS} vs V_{DS} for JNTs with different W_{fin} at 300K, with gate voltage overdrive ($V_{GT}=V_{GF}-V_T$, where V_T is the threshold voltage) of 1V. As shown by these curves, for $V_{DS} < 0$ the current is significantly more linear than for positive V_{DS} values, where the linearity is limited by the saturation of current, which dominates the device global nonlinearity.

Generally, HD properties of MOSFETs are dominated by the second-order harmonic. However, in applications such as MOSFET continuous-time filters, balanced structures are used (2), in order to suppress the even-order harmonics, such that the third-order harmonic (HD3) becomes dominant. The distortion characteristics have been obtained using the IFM method (6), which allows for accessing the HD through DC measurements. For this analysis, devices have been biased at V_{DS}=0V and the sinusoidal signal amplitude is varied. The obtained HD3 with signal amplitude of 100 mV is presented in Fig. 3 as a function of V_{GT}, for JNTs at 300K. As shown in this figure, V_{GT} increase improves the linearity, as it increases the saturation voltage. In practice, low V_{GT} values are not of interest when transistor is used as quasi-linear resistor, but only as an amplifier, that operates in saturation. The reduction of W_{fin} has shown to slightly worsen HD3. Also, a negative peak is observed around V_{GT}=800mV, marking the transition between saturation and linear regions. A displacement of this peak is observed when the temperature increases, as shown by the curves of W_{fin}=20nm at different T, also presented in Fig. 3. No clear tendency of HD3 with T has been observed. The obtained HD3 is lower than those reported in ref. (7) for IM Triple gate devices (around -70 dB for W_{fin}=30nm at V_{GT}=1V, signal amplitude of 100mV and 300K).

From the curves of Fig. 2, R_{ON} has been extracted with V_{DS}=100mV as a function of W_{fin} and is presented in left axis of Fig. 4. The fin narrowing causes R_{ON} increase at 300K. Extracted R_{ON} is also presented as a function of T for JNTs with W_{fin}=20 and 30nm. As shown, R_{ON} does not present a monotonic tendency with T. In conventional IM transistors, T rise causes R_{ON} increase due to mobility reduction. This tendency can be also seen for JNT only for T ≥ 450 K approximately. Below this T, R_{ON} starts increasing again, which may be due to incomplete ionization of dopants in silicon layer that has been already shown to play an important role in JNTs resistance even when working above cryogenic regime and near 300 K (8, 9).

Conclusions

In this work the performance of JNTs as quasi-linear resistor has been presented for the first time. Unlike from IM transistors, where the on-resistance monotonically increases with temperature rise, the resistance of JNTs has shown a 'valley' around 450K, increasing below this temperature. This increase may be related to incomplete ionization, which is important in these kind of devices. It has been observed that the third-order harmonic distortion is slightly worsened by W_{fin} increase, although it is smaller than the values reported in the literature for IM Triple gate devices with similar W_{fin}.

Acknowledgements

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References

(1) A. Cerdeira et al, IEEE Trans On Electron Dev, v. 52, p. 967 (2005).
(2) L. Vancaille et al , IEEE Trans On Electron Dev, v. 53, p. 263 (2006).
(3) J.-P. Colinge et at, Nature Nanotechnology, v. 5, p. 225 (2010).
(4) R. T. Doria et al, IEEE Trans On Electron Dev, v. 58, p. 2511 (2011).
(5) R. T. Doria et al, ECS Transactions, v. 2, p. 13 (2010).
(6) A. Cerdeira et al, Solid-St Electron, v. 48, p. 2225 (2004).
(7) R. T. Doria et al, Solid-St Electron, v. 62, p. 99 (2011).
(8) R. T. Doria et al, Journal of Int Circ and Syst, v. 7, p.121 (2012).
(9) R. D. Trevisoli et al, Appl. Phys. Lett. 101, 062101 (2012).

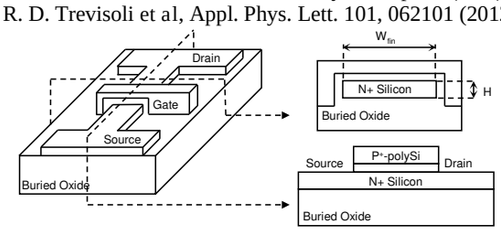

Fig. 1 – Schematic view of the silicon nanowire MOSFET and cross-sections of a junctionless nMOS transistor.

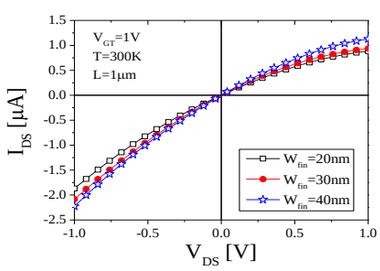

Fig. 2 – I_{DS} vs V_{DS} curves in linear operation regime, at V_{GT}=1V and 300K.

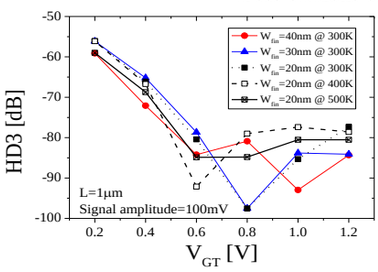

Fig. 3 – HD3 as a function of V_{GT} for JNTs with different W_{fin} and temperature.

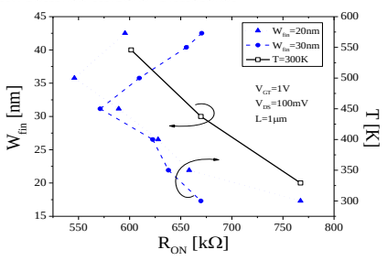

Fig. 4 – Calculated R_{ON} as a function of W_{fin} and temperature at V_{GT}=1V and V_{DS}=100mV.