Analog Behavior of Submicron Graded-Channel SOI **MOSFETs Varying Channel Length, Doping Concentration and Temperature**

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Introduction

Graded-Channel (GC) SOI nMOSFET (1) was proposed and demonstrated to reduce the high electric field in the region near the drain, efficiently improving the analog characteristics of SOI transistors both at device and circuit level (2,3,4,5,6). This device presents an asymmetric doping concentration in the channel, which is divided in two regions, a highly doped (HD, with doping level NAH) one near the source, responsible for fixing the device threshold voltage (Vth), and a lightly doped (LD and doping level NAL) one near the drain, with length LLD. The LD region decreases the potential barrier in the channel-to-drain junction, reducing the impact ionization. In this paper the analog performance of Graded-Channel (GC) SOI nMOSFETs with deep submicrometer channel length is investigated, as a function of total (L) and light doped region $(L_{\rm ID})$ length, doping concentration and temperature, starting from an industrial 150 nm fully depleted (FD) SOI technology. The obtained results show that larger improvement of the intrinsic gain voltage occurs when the length of the lightly doped region is approximately 100 nm regardless the total channel length, doping concentration and temperature.

Results and Discussion

Graded-Channel SOI nMOSFETs measured in this study features $t_{Si} =$ 40nm, $t_{oxb} = 145$ nm, $t_{oxf} = 2.5$ nm, $V_{th} = 0.6$ V at room temperature and were fabricated in a 150 nm FD technology from OKI Semiconductors (7). Two-dimensional numerical simulations of the process flow were executed varying both L, L_{LD}, doping concentration at the HD side (N_{AH}) and temperature using Sentaurus simulator (8). An experimental GC device with channel width (W) of 240 µm and L=0.5µm, with $L_{LD}/L=0.5$ was used to adjust the model parameters(9). Mobility degradation due to lateral and vertical electrical fields, doping dependent carrier lifetime and bandgap narrowing models were included in all simulations.(). Figs 1 and 2 show comparisons between simulated and measured drain current (I_Ds) curves, as function of gate voltage (V_GF) with drain-to-source voltage (V_{DS}) of 1V and as a function of V_{DS} with $V_{GI}=V_{GF}-V_{th}=300$ mV, respectively. The output conductance (g_D) and transconductance (gm) are also presented. Good agreement has been obtained between the experimental and simulated curves and their first



Fig. 1.: Simulated and Measured I_{DS} and g_m curves as function of V_{GF} of GCSOI with L=500nm, V_{DS} =50mV, L_{1D}/L =0.5.



Fig. 2.: Simulated and Measured I_{DS} and g_D curves as function of of GCSOI with L=500nm,V_{GT}=0mV V_{r} and $300mV, L_{1D}/L = 0.5.$

derivatives. After adjusting model parameters, numerical simulations were performed for GC SOI MOSFETs varying L. LLD/L ratio, NAH and T. Figure 3 presents g_D as a function of L_{LD} for devices with two N_{AH} and L values. The g_D values extracted at V_{GT} =200mV and V_{DS} =1V are presented in figure 3. The values of $L_{LD}/L=0$ refer to an uniformly (conventional) SOI device. The results show that g_D decreases with LLD increase, due to the reduction of electric field and hence channel length modulation (CLM) effect. Nevertheless, for longer LLD values with consequent Leff reduction, CLM becomes more pronounced, degrading the output conductance from $L_{LD} > 150$ nm approximately. On the other hand, the simulated results show that gm always increases with L_{LD} increase. These results directly affect the intrinsic voltage gain ($A_V=g_m/g_D$)), presented for the same devices in Fig. 4. From this figure one can note that the most interesting results for Av were obtained for a lightly doped region length (L_{LD}) of about 100 nm regardless N_{AH} total L. For devices with N_{AH} = 2x10^{1/}cm⁻² and $N_{AH} = 2 \times 10^{18} \text{ cm}^{-3}$, the maximum A_V of 59. dB and 68 dB have been observed, respectively, both at L_{LD} =100 nm. Fig. 5 presents A_V vs L_{LD} varying N_{AH} for devices with L=240nm, showing that the larger doping concentration levels lead to Av increase.

In Fig. 6 its possible to note that even with T change, the maximum A_V remains also with L_{LD} in the order of 100nm, following g_D behavior. In addition, the lower T the better the Av results, due to gm increase that overcomes the gD degradation caused by T lowering.

Conclusions

In this paper experimentally calibrated numerical simulations were used to investigate the GC SOI analog characteristics as function of the L, L_{LD}/L, N_{AH} ratio and T. It has been found that the increase of NAH promotes the reduction of gD, which combined with the larger gm is responsible for the larger intrinsic voltage gain (Av). The most interesting results for Av were obtained for L_{LD} = 100 nm regardless N_{AH} and L. Concerning the temperature, it has been observed that its decrease leads to larger A_V, whose maximum value remains at L_{LD}=100nm.

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Fig. 3.: Extracted g_D as function of L_{ID} varying L and N_{AFb} with $V_{DS}=1V$ and $V_{GI}=200mV$.







L_[nm] Fig. 5.: Extracted g_D as function of L_{LD} varying N_{AH} with $V_{DS} = 1V V_{GT} = 200 mV$, L=240nm



