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Thickness Dependent Electrical Characteristics of InAlN/GaN-on-Si MOSHEMTs with Y_2O_3 Gate Dielectric and Au-free Ohmic Contact

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Lattice matched InAlN/AlN/GaN heterostructure offers higher charge density for thin barrier thicknesses (< 10 nm) due to stronger polarization discontinuity than the conventional AlGaN/GaN heterostructure for future power and RF devices with low power consumption [1-2]. In addition to the excellent material properties, GaN-on-Si wafers opens up a new flexibility to be able to compete with Si power devices in terms of cost. Meanwhile, gate leakage current is an important factor that limits the performance and reliability of conventional high-power devices. Hence, a thin dielectric oxide layer is often inserted between the gate metal and the InAlN barrier layer leading to the approach of the MOS HEMT.

Likewise, in addition to enabling device fabrication in Si fabs, a Au-free metallization scheme is also need to be addressed. Therefore, the present work focuses on the MOSHEMT fabrication choosing Y_2O_3 as a gate dielectric and Ti/Al/Ni/W system as an initiative to address Au-free technology compatible for Si fab industry.

The lattice-matched $In_{0.18}Al_{0.82}N$/AlN/GaN HEMT structure used in this experiment was grown by metal–organic chemical vapor deposition on high resistive Si (111) substrate, the details of which are shown schematically in Fig. 1. The MOSHEMT device fabrication process started from mesa isolation by inductively coupled plasma etching using Cl_2/BCl_3 gases. Then, a Ti/Al/Ni/W layer was sputter deposited followed by rapid thermal annealing at 900 °C for 60 s in vacuum to form Au-free source and drain ohmic contacts. Subsequently, different thicknesses of Y_2O_3 ultra-thin films (5-30 nm) were deposited using pulsed laser deposition (PLD) with KrF excimer laser. Thereafter, W was sputter deposited to form the gate contact. The devices were annealed at several temperatures ranging from 400-500 °C in N_2 ambient. The device was passivated with SiN grown by plasma enhanced chemical vapor deposition (PECVD).

The contact resistance components for Ti/Al/Ni/W ohmic contacts were analyzed based on the transmission line method (TLM). From the TLM patterns, a total contact resistance of 0.35 Ω·mm and a contact resistivity of 1.03×10^{-6} Ω·cm^2 were extracted. The devices with W/L= 100/2 µm were used for DC output and transfer characterization. Figure 2 (a) shows the measured transfer characteristics, I_{ds}-V_{gs} of MOSHEMTs having different Y_2O_3 film thicknesses, range between 5-30 nm. It is worth noting that strong thickness dependence shift in threshold voltage, V_{th}, has been observed. In fact, a positive shift in V_{th} has been noticed with lower Y_2O_3 film thickness, which could be due to the formation of more interface/bulk negative charges. The 5 nm thick Y_2O_3 film during as-deposited condition demonstrates enhancement mode device performance having a positive V_{th} (+0.31 V). Moreover, strong annealing temperature dependent V_{th} shifts have also been observed, as shown in Fig. 2(b). Indeed, more negative shifts in V_{th} with increasing annealing temperature have been observed for all film thicknesses. However, the peak extrinsic transconductance is found to improve from ~70 mS/mm to ~110 mS/mm for increase in Y_2O_3 film thickness from 5 to 30 nm (data not shown), while the maximum saturation drain current, I_{dsat}, is noticed to improve 17.6 % further at the same V_{gs} likely due to higher overdrive voltage for 30 nm film thickness compared to that of 5 nm, as shown in Fig. 3. The positive shift in flatband voltage, V_{fb} with lower Y_2O_3 film thickness is also evidenced from the capacitance-voltage measurements, as shown in Figs 4. The dielectric permittivity is found to improve from 14.9 to 17.6 subject to thermal annealing at 450 °C in N_2.

In conclusion, thickness dependent electrical performances of InAlN/GaN MOSHEMTs-on-Si with Y_2O_3 gate dielectric have been investigated. A positive shift in threshold voltage with lower film thickness while an improved transconductance and maximum saturation drain current have been obtained for thicker film thickness.

Acknowledgement
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References
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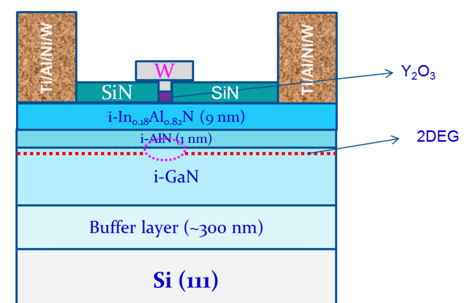

Fig. 1: Schematic illustration of fabricated MOSHEMT with Y_2O_3 gate dielectric and Au-free ohmic contacts.

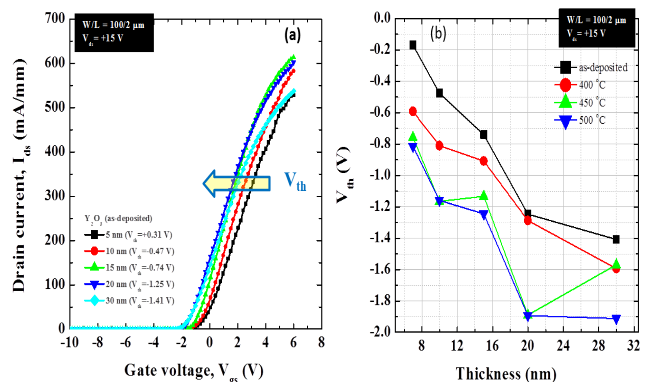

Fig. 2: (a) Thickness dependence and (b) annealing temperature dependence transfer characteristics of Y_2O_3 MOSHEMTs on InAlN/GaN-on-Si.

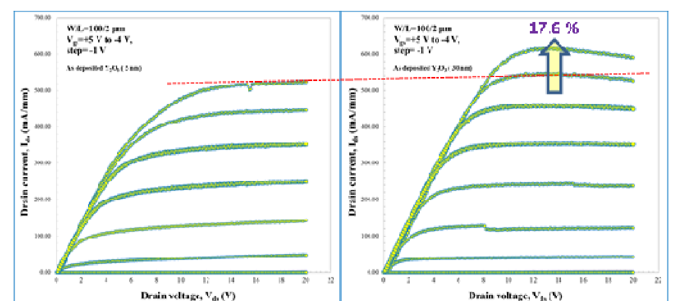

Fig. 3: A comparison of measured I_{ds}-V_{ds} characteristics of MOSHEMTs with two different Y_2O_3 film thicknesses.

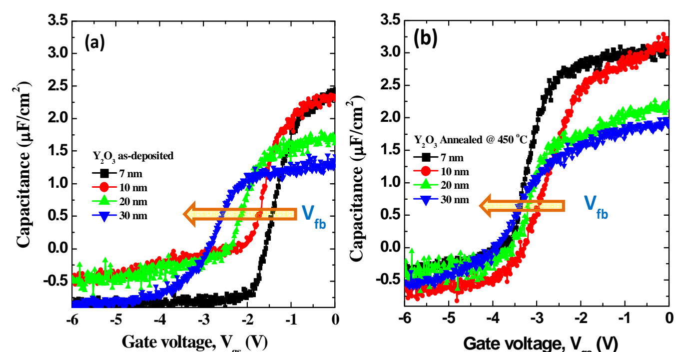

Fig. 4: Measured capacitance-voltage characteristics of Y_2O_3 MOSHEMTs (a) without and (b) with thermal annealing.