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Stress Simulations of Ge-Based FinFET devices

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With the arrival of FinFET architectures, yet another level of complexity has been added to high-performance CMOS technologies [1,2]. While for planar architectures, development of nFETs and pFETs was already challenging due to the interaction of stress techniques and gate-last schemes in dense layouts, the added topography of FinFETs increases the number of optimization variables even further. Moreover, future nodes will become more complicated as silicon-channels may be replaced by high-mobility materials like Ge/SiGe or III/V-semiconductors. As it is impossible to develop and evaluate these diverse technologies through experiments alone, TCAD is indispensible for the first assessment and understanding of the various interactions affecting the performance. The purpose of this work is to highlight some challenges and opportunities when integrating different stress techniques in scaled, dense, gate-last FinFETs with silicon- or germanium-channels. Six stressor types are compared: Strain-Relaxed Buffers (SRBs), source/drain (S/D) stressors, strained Contact-Etch Stop Layers (CESL), and intrinsically stressed gate liners, gate-fill, and contacts.

While in planar technologies SRB's deliver a very high biaxial stress in the channel, in FinFETs it leads to *uniaxial* longitudinal stress due to the fin's aspect ratio. For pFETs, uniaxial stress is preferred over biaxial, making SRB's an attractive booster, especially for Ge-channels where the required compressive strain can be generated through a $Si_{1-x}Ge_x$ SRB. This is confirmed by the mobility enhancement plotted in Figure 1: SRB's are found to be the most efficient boosters for 14 nm-node (DR14) Ge p-FinFETs, followed by S/D stressors.

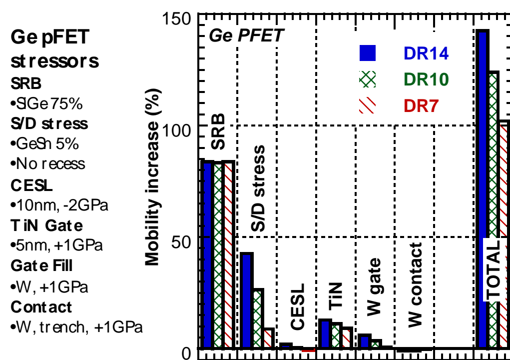

Figure 1. Mobility enhancement of different stressors for Ge p-FinFETs with 14, 10 and 7 nm node dimensions (DR14-DR10-DR7). A scaling scenario is assumed whereby the poly and fin pitches are scaled by a factor of 0.7 per node, but the gate length only by a factor of 0.9.

Moreover, SRB's show good scalability from the 14 nm node to the 10 nm (DR10) and 7 nm (DR7) nodes. Figure 1 shows a scaling scenario where the poly and fin pitch are ideally scaled (x0.7 between nodes), while the gate length is scaled less aggressively (x0.9 per node) due to short-channel effects. As the space between gates decreases strongly from one node to the next, the S/D stressor becomes largely ineffective in DR10 and DR7. The SRB however retains its mobility enhancement down to the 7 nm-node.

When the channel is already strained by the underlying SRB, the recess etch of a S/D stressor module will partially release the channel stress generated by the SRB ("After S/D etch", Figure 2). Although the channel stress can then be recovered by growing the S/D epitaxial layer and by removing the gate (Figure 2, right), it is found that, when combining an SRB and a S/D stressor, the highest mobility boost can be achieved by omitting the S/D etch altogether and opting for a raised S/D stressor, Figure 3. However, in the absence of an SRB, a deeper recess of the S/D module leads to more improvement, Figure 3 (right). Similar optimizations between SRBs and S/D stressors have been reported for planar FETs [3-4].

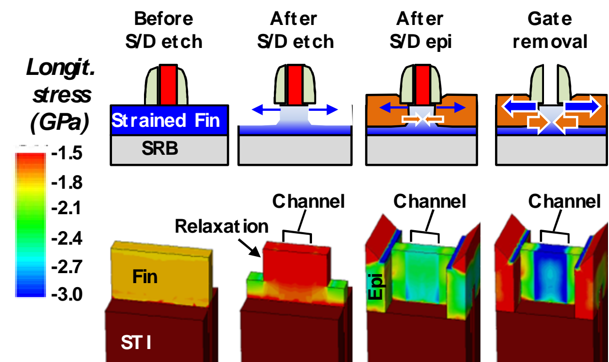

Figure 2. (Top) Schematic and (bottom) longitudinal stress contours after different process steps of a gate-last p-FinFET process with 14 nm-node dimensions. The results show a Ge channel with a SiGe75% SRB, and a GeSn5% S/D stressor with 20 nm recess etch of the fin. The bottom figures show only Ge, SiGe, GeSn S/D and SiO_2 regions, the gate stack and spacers have been omitted from this view.

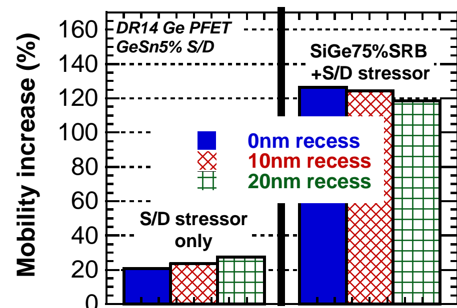

Figure 3. Mobility increase for Ge p-FinFETs with 14 nm-node dimensions for a GeSn5% S/D stressor, in the absence of an SRB (left), and when combined with a SiGe75% SRB (right).

Besides the aforementioned results, further considerations will be provided on mobility optimization, comparing Ge and Si-channels as well as pFETs and nFETs. It will be shown how SRB and S/D stressor effectiveness can be exchanged for these transistors, moreover the difference in sensitivities to stressors for Ge FETs and Si FETs will be highlighted.

References

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[4] Eneman G. et al., Proceedings of SSDM (2012).