

Fin Dimension Influence on Mechanical Stressors in Triple-Gate SOI nMOSFETs

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Preliminary Data and Discussions

Unstrained and strained triple-gate SOI devices under different strain techniques are studied experimentally and by simulations. As devices scale down, the fin width influence on the different strain techniques is analyzed through 3D process simulations and experimental results. The experimental devices are triple-gate SOI n-MuGFETs fabricated at imec, Belgium. The channel doping level is $N_A=1 \times 10^{15} \text{cm}^{-3}$, the fin height is 65nm and the gate dielectric is composed of 2.3nm HfSiON (50% Hf) on 1nm SiO₂. The midgap metal gate is obtained by deposition of a 5nm TiN layer and 100nm thick polysilicon capping to complete the gate electrode. Three types of mobility boosters are applied on the devices: a strained Si layer epitaxially grown on a r-Si_{0.8}Ge_{0.2} strain-relaxed buffer (SRB), an uniaxial strain obtained using the tensile strained contact etch stop layer (tCESL) technique (1), by depositing a 100nm thick nitride layer and the both methods tCESL + SiGe SRB combined. Devices have fin widths (W_{Fin}) of 20 and 870nm and a channel length (L_{ch}) of 150nm. The structures obtained through the 3D process simulation reflect the dimensions of measured experimental devices. Fig. 1 and 2 present the simulated strain components in the vertical and longitudinal directions respectively, for the three types of strain. They are extracted vertically in the center region of the fin. The tensile strain in nMOSFETs causes, among other changes, a reduction of the bandgap, a lowering of the effective electron mass and reduces the scattering ratio of electrons, beneficial to the carrier mobility. Fig. 3 shows the maximum transconductance from experimental data ($g_{\text{m,max}}$) in the upper left panel with $V_{\text{DS}}=50\text{mV}$, normalized by W_{eff}/L (where $W_{\text{eff}}=W_{\text{Fin}}+2*H_{\text{Fin}}$), and in the upper right panel the $g_{\text{m,max}}$ enhancement due to the strain compared to unstrained devices (reference) is shown. The global electron mobility is extracted from experimental data following the Y-method (2), shown in the lower left panel, while the mobility enhancement obtained with the use of the strain with respect to the reference is shown in the lower right panel of Fig. 3. The longitudinal strain from SiGe SRB presents a uniform distribution in the channel area along the fin height with $W_{\text{Fin}}=20\text{nm}$ having higher strain than $W_{\text{Fin}}=870\text{nm}$. The

tCESL technique delivers a non-uniform longitudinal strain distribution along the fin height. The non-uniformity in longitudinal strain increases in the narrow fin $W_{\text{Fin}}=20\text{nm}$ and is higher near the buried oxide interface. The combined strain returns the sum of both strains in values. However, for the normalized $g_{\text{m,max}}$ the tCESL returns 84.5% and 42.2% improvement over reference devices for $W_{\text{Fin}}=20\text{nm}$ and 870nm respectively, against 58.8% and 16.2% respectively in the SiGe SRB stressor. The combined strain delivers the highest enhancement with 103.7% for $W_{\text{Fin}}=20\text{nm}$ and 46.4% for $W_{\text{Fin}}=870\text{nm}$. The electron mobility delivered by reference devices, with $170.8\text{cm}^2/\text{Vs}$ and $158.8\text{cm}^2/\text{Vs}$ for $W_{\text{Fin}}=20\text{nm}$ and 870nm respectively, lies near the range of values observed in reference (3), using similar FinFETs. The gate-to-channel electrostatic coupling and the carriers distribution for $W_{\text{Fin}}=20\text{nm}$ may turn the global electron mobility higher in this device than for $W_{\text{Fin}}=870\text{nm}$, even with the larger current flowing in the top of the $W_{\text{Fin}}=870\text{nm}$ fin due to the (100) orientation. For $W_{\text{Fin}}=20\text{nm}$ the mobility's behavior matches the normalized $g_{\text{m,max}}$, with gains of 61.5% for SiGe SRB stressor, 84.8% for tCESL and 159.8% for the combination. However, for $W_{\text{Fin}}=870\text{nm}$ the mobility in SiGe SRB shows only 22.7% enhancement staying at $194.9\text{cm}^2/\text{Vs}$ and the tCESL returns $369.4\text{cm}^2/\text{Vs}$ of electron mobility, resulting in 132.6% improvement. However, the electron mobility in the combined stressors decays below the tCESL values, remaining at $341.5\text{cm}^2/\text{Vs}$ with 115.1% of enhancement, a different trend from what was expected based on normalized $g_{\text{m,max}}$.

Remarks and Further Analysis

The lack of expected enhancement for $W_{\text{Fin}}=870\text{nm}$ with combined stressors is supposed to be linked to process issues, maybe related to the SiGe SRB as this stressor itself led to lower than expected electron mobility. The transconductance and mobility data collected show global values and not crystallographic orientation specific. Further study will be done to obtain the $g_{\text{m,max}}$, electron mobility and strain in the top and sidewalls separately and the investigation will enlighten the differences existent in the global electron mobility dependent on crystallographic orientation connected to the different mechanical stressors methods and the strain generated in the main planes of current conduction.

References

1. N. Collaert et al., VLSI Symp. Tech. Dig., p.52, 2006.
2. G. Ghibauda, Elec. Letters, v.24, no.9, p.543, 1988.
3. T. Rudenko et al., Micr. Eng., v.80, p.386, 2005.

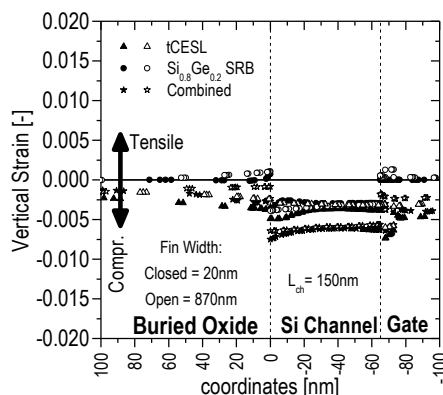


Fig. 1. Vertical strain

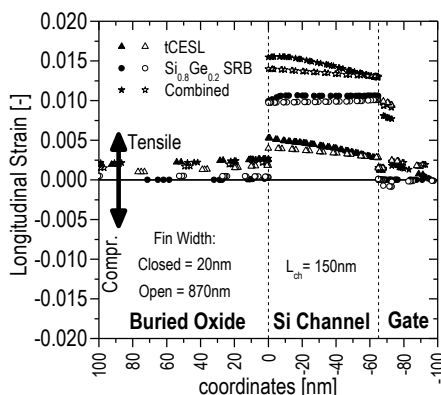


Fig. 2. Longitudinal strain

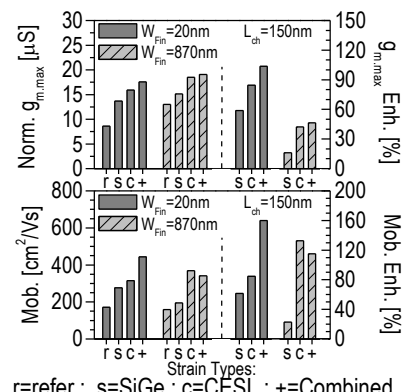


Fig. 3. Transconductance and mobility