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The past, present and future of high-k/metal gates

Kisik Choi, Takashi Ando*, Martin Frank*, Eduard Cartier*, Vamsi Paruchuri**, John Iacoponi, Vijay Narayanan*

GLOBALFOUNDRIES at IBM T. J. Watson Research Center, Yorktown Heights, New York, 10598

**IBM T. J. Watson Research Center, Yorktown Heights, New York, 10598*

***IBM Albany NanoTech Center, Albany, New York, 12203*

Gate stacks with high-k/metal gate has been a key enabler of the high performance and low power MOSFET device evolution for the past several technology nodes by lending superior electrostatics for short channel control, along with low gate leakage current [1]. There are two major fabrication schemes to construct high-k/metal gate structure; gate-first and gate-last. Each scheme relies on unique mechanism to obtain desirable device parameters such as work function. Each scheme has its own pros and cons but both made their ways to move on to mass production by several manufacturers. Gate-first approach allowed easier migration from Poly/SiON and provided nice Tinv scaling capability [2-4] while gate-last approach is known to utilize eSiGe stress more efficiently by removing poly-Si [5]. Despite the structural differences, the mechanisms governing device reliability are somewhat universal for both high-k/metal gate schemes and Tinv scaling has been severely challenged by the reliability, especially NBTI [6]. Recent introduction of multigate FET devices into production could be partially explained by the limitation of the Tinv scaling originated by the reliability constraints [6]. Multi-gate structure itself can provide superior short channel control so that it can compensate the lack of Tinv scaling. It is projected that the next device scaling is likely to come from operation voltage scaling. High mobility channel materials such as Ge and III-V are considered to be implemented because those materials could provide higher performance at a scaled operation voltage [1]. As the conventional, almost linear gate scaling changes its course to somewhat diverging scaling path, high-k/metal gate should evolve accordingly to fulfill the ever challenging requirements of the new device architectures. In this talk, the evolution of high-k/metal gate stack will be reviewed and the conditions required for the future high-k/metal gate will be discussed.

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