Determination of Effective Capacitance Area for Pseudo-Transistor based Characterization of bare SOI wafers by Split-C(V) measurements

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The split-C(V) technique has served during three decades for independent extraction of the inversion and accumulation charge in MOSFETs from the direct measurement of the gate-to-channel capacitance [1]. The total charge, Q, obtained from the integration of the gate-to-channel capacitance curves, can be used for the evaluation of the carrier mobility using the standard MOSFET equations ($\mu \alpha I_D/Q$). Recently, the Split-C(V) technique has been applied for the first time to the characterization of carrier mobility in bare SOI wafers using the Pseudo-MOSFET configuration (Figure 1.a). This experimental setup avoids the need for a CMOS processing to obtain mobility vs. inversion charge curves [2-3]. However, there are some particularities associated with the Pseudo-MOSFET configuration when performing split-C(V) measurements that are not present in a regular MOSFET and need to be further investigated:

i) the area is not defined by the gate rectangle; in contrast, the spreading of the carriers in the silicon film yields, due to the milimetric size of the device, a strong frequency dispersion of the C-V curves measured using an impedance analyzer (Fig. 1.b), and

ii) the distance between the needles plays an important role since it becomes comparable with the size of the MESA-isolated silicon film [6]; therefore the area covered by the carriers contributing to the gate-to-channel capacitance may vary with the needle interdistance, d, or with the number of needles on the surface (Fig. 2.a).

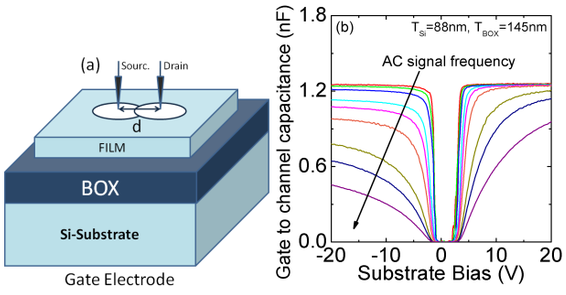

Fig1. (a) Schematic of the Pseudo-MOSFET configuration: two needles are applied on the wafer surface acting as source and drain electrodes separated by a distance d, whereas the wafer substrate acts as the transistor gate. **(b)** Gate-to-channel capacitance curves obtained in Pseudo-MOSFET configuration showing the frequency dispersion when the frequency of the AC signal in an Agilent 4294A is varied; f=300, 500, 1k, 3k, 5k, 10k, 30k, 50k, 100kHz.

The precise effective capacitance area of the Pseudo-MOSFET can be calculated assuming that each needle creates a circular shaped region (effective capacitance circle) were the carriers are able to follow the AC signal as illustrated in Figure 1.a. From geometrical relationships the following expression is obtained for this area:

$$S_{eff} = \gamma r_{eff}^2 \left(2\pi - k\left(2\arccos\left(\frac{d}{2r_{eff}} \right) \right) - \sin\left(2\arccos\left(\frac{d}{2r_{eff}} \right) \right) \right) \quad (1)$$

where γ is a factor calcualted analytically depending on the needle separation, size of the cell and potential drop from the needle to the edge of the circles where the carriers can follow the AC signal. r_{eff} is the radius of the effective capacitance circles induced by the needles and can be obtained combining quasi-static capacitance measurements (QSC) [5] and AC measurements. k is a constant accounting for the overlap of the effective capacitance circles in two-needle configuration. The previous expression (1) can be easily expanded for an arbitrary number of needles aligned on the wafer surface.

The importance of the proper determination of the area for the extraction of the mobility is clearly manifested in Figure 2.b. The Split-C(V) technique was applied to an SOI wafer with a passivated surface [4]. A thick BOX of 145nm was selected to avoid the influence of the dielectric relaxation of the carriers at the substrate-BOX interface [6]. The results in solid-line correspond to mobility obtained when the area is calculated by the proposed model, whereas dashed lines are extracted by assuming the separation of the needles, d, and the geometrical factor of the Pseudo-MOSFET ($W/L=0.75$) [7] as criteria for the area calculation.

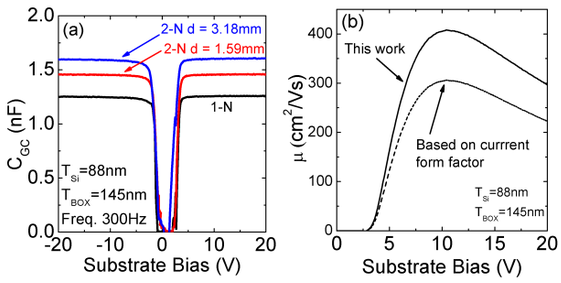

Fig 2. (a) Gate to channel capacitance curves obtained for one needle on the surface, and two needles separated $d=1.59mm$ and $d=3.18mm$. **(b)** Experimental mobility extracted obtained by applying the split-C(V) technique to a passivated $T_{Si}=88nm$, $T_{BOX}=145nm$ SOI wafer. The use of inappropriate effective area for the calculation (dashed line), may lead to an underestimation of the carrier mobility (electrons in the case showed). In contrast, the actual mobility obtained by using the more accurate model proposed in Eq. 1 is 30% larger.

A 30% of mobility underestimation is generated by the inadequate area determination. As we will show, this type of error may lead to incorrect conclusions regarding the film or interface quality especially in ultra-thin silicon films.

Acknowledgemets

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