Semi-metal nanowire field effect transistors from first principle calculations

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Bandgap engineering in semimetal nanowires can be utilized to form a field effect transistor (FET) near atomic dimensions and eliminates the need for doping in the transistor's source, channel, or drain. For sufficiently small wire diameters the metallic behaviour of the semimetal is lost and a bandgap is induced. Using a full quantum mechanical description of the semimetal nanowires, we are able to demonstrate that the design of a dopant-free, monomaterial confinement modulated gap transistors (CMGT) which unlike conventional FETs does not require dopant atoms to define different device regions. This overcomes a primary obstacle to fabricating sub-5 nm transistors, enabling aggressive scaling to near atomic limits.

Nanoscale FETs enable the continuation of the Moore's law for future technology generations, permit higher device density and consequently high function per integrated circuit at lower unit cost. Critically, use of nanowire transistors permits efficient electrostatic control over charges in the nanowires to allow for low power nanoelectronics.

Gray tin (Sn) has a diamond cubic structure with a zero bandgap [1,2], ie it is a semi-metal. In this work, we performed atomic scale simulation using DFT to study the electronic structure of Sn nanowires with different crystallographic orientations and assess the effects of nanowire diameter on the electronic structure. Based on the different electronic properties of Sn in both bulk and nanowire forms, we propose a new structure for FETs which is compatible with current silicon-based nanofabrication technology.

At small nanowire diameters, the formation of a bandgap is attributable to the well known phenomena of quantum confinement. The CMGT is comprised of a metallic source and drain, and intrinsic semiconducting tin nanowire with 1 nm diameter as a channel with a bandgap of 1.58 eV [2]. The source-drain regions are constructed from larger cross-section tin nanowire (diameter of 4 nm) to create metallic drain as is shown in Fig. 1. To improve the electrostatic control of the gate over the channel, a gate-all-around configuration has been introduced into the structure [3]. The oxide surrounding the nanowire is modeled as a continuum material described by a thickness of 1 nm and with the dielectric constant of hafnium oxide $\varepsilon_{HfO2} = 25$.

To investigate the device performance, the electronic transmission and, hence, the current is calculated from the first-principles using Hamiltonian in the DFT implementation with the method of the non-equilibrium Green's function (NEGF) [4]. The Hamiltonian in the DFT implementation chosen in this study is constructed in terms of a localized basis set. This local character allows the device region to be partitioned into left lead, right lead and scattering (channel) region. Electron transport is described within the Landauer formalism for the CMGT based on the assumption that the transport along the channel region is coherent [5]; i.e., inelastic scattering is negligible within the short length of the channel whose resistance is dominated by the interface to the larger cross sectional areas of the source and drain, as can be deduced from the local density of state shown in Fig. 2(a). The channel-source and -drain junctions are Schottky barriers as depicted in Fig. 2(b).

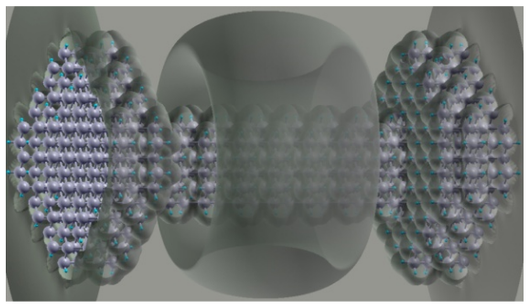
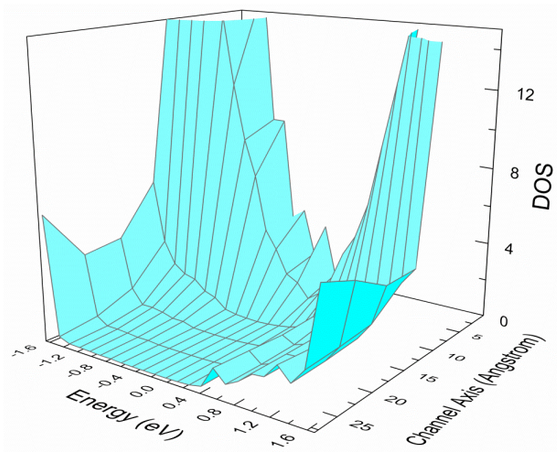
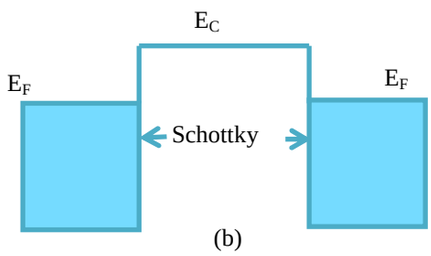


Fig.1. Atomic scale illustration of CMGT. The ring around the channel region indicates an isopotential surface due to the applied gate bias.



(a)



(b)

Fig. 2. (a) Local density of state along the channel axis versus energy for different atomic layers in equilibrium. The energies are referenced to Fermi level. (b) Energy band diagram in leads and channel regions.

The drain−source current voltage characteristic of CMGT shows that the subthreshold slope and the on/off ratio of 72.6 mV/dec and up to 10^4, respectively, can be achieved.

References

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