

Strain Engineering in Fully Depleted SOI MOSFETs: Is Bulk FinFET the Only Path to High Performance?

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Fully depleted MOSFETs are considered as the technology driver in 14nm node and beyond due to limitations of planar CMOS in controlling short channel effects and increased importance of device variability. In a fully depleted device such as extremely-thin SOI (ETSOI) or FinFET, short channel effects are controlled by the virtue of very thin channel, while threshold voltage variations can be lowered by keeping the channel undoped or lightly doped.

While ETSOI, SOI FinFET, and bulk FinFET provide similar benefits in terms of improved short channel control, the common belief in the semiconductor industry is that bulk FinFET is the only path to high performance as it allows the use of embedded stressors. We will demonstrate that this is to a large extent exaggerated and not supported by hardware data. Moreover, as the device pitch is scaled in future technology nodes, the effectiveness of embedded SiGe drops significantly. Channel strain engineering where the channel material is intrinsically strained will be more effective in future and is in principle independent of the device pitch. In this case SOI technology offers significant advantage to incorporate different strained channel materials.