Gold-free InAlN/GaN Schottky Gate HEMT on Si (111) Substrate with ZrO_2 Passivation

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Introduction

InAlN/GaN High Electron Mobility Transistors (HEMTs) are promising candidates for high speed and high power applications owing to its high thermal stability and high Two Dimension Electron Gas (2DEG) concentration [1]. However, cost is the challenge for InAlN/GaN HEMT to compete with other semiconductor devices. By growing InAlN/GaN HEMT structure on Si substrate for economy of scale and developing Si compatible fabrication processes to allow the making of InAlN/GaN HEMT in current Si fabrication foundries would make InAlN/GaN HEMTs more cost competitive. Traditional contacts of InAlN/GaN HEMTs are gold based, which are not welcome in Si fabrication foundries as gold is a deep level trap for Si and is very diffusive in Si, which can degrade the Si device performance. Therefore, we aim to develop non-gold based contacts for InAlN/GaN HEMTs to reduce the cost and in this paper, we report our investigations on gold-free InAlN/GaN Schottky gate HEMT on Si (111) substrate with ZrO_2 passivation. The source/drain ohmic contacts are Ti/Al/Ni/W and the gate metal is Ni/W.

Experimental Procedures

The ohmic property of gold-free Ti/Al/Ni/W contacts was investigated by means of the Transmission Line Method (TLM) structure. Schottky diodes with different Ni/W thickness ratios (50/50, 150/50, 250/50, 350/50 nm) were fabricated to investigate the Schottky barrier height (SBH) of Ni/W on InAlN/GaN under different annealing temperatures (200, 400 and 600 ^oC). We used InAlN/GaN HEMT structure grown on 4-inch Si (111) substrate and fabricated 2 µm gate length Ni/W Schottky gate HEMTs with Ti/Al/Ni/W source/drain contacts. The sheet resistance of the InAlN/GaN HEMT structure was found to be 600 Ω/□ using Hall measurements. Mesa isolation of HEMTs was etched by inductively coupled plasmas using BCl_3/Cl_2 gases. After mesa isolation, Ti/Al/Ni/W source/drain contacts were sputter deposited, followed by annealing at 900 ^oC for 1 minute in vacuum. Prior to gate metal deposition, O_2 plasma surface treatment was performed. The Schottky gate contact (Ni/W) was then sputtered. Finally, a very thin 7 nm dielectric, ZrO_2, was deposited using Atomic Layer Deposition (ALD) for device passivation.

Results and Discussion

Ti/Al/Ni/W on InAlN/GaN has a minimum contact resistivity (ρ_c) of $1.03x10^{-6}$ Ωcm^2 and contact resistance of 0.35 Ωmm when annealed at the temperature of 900 ^oC for 1 minute in vacuum. As shown in Fig. 1, SBH of Ni/W on InAlN/GaN increases with increasing Ni/W ratio. In Fig. 2, as the annealing temperature increases, the reverse leakage current increases while the forward bias current and SBH improves. Above 600 ^oC, the leakage current increases and Schottky contact degrades. The optimum annealing temperature for Ni/W Schottky gate on InAlN/GaN was found to be 400 ^oC. Maximum SBH of 0.72 eV and ideality factor of 2.97 were achieved. Relatively low SBH and high ideality factor are due to the domination of tunneling current through the dislocation defects in InAlN layer, as discussed in the work of Donoval [2]. Clear advantage is observed using a thin 7 nm ZrO_2 layer to passivate InAlN/GaN HEMTs, as shown in Figs. 3. Devices without passivation achieve a maximum g_m of 120 mS/mm and R_{on} of 12 Ω/mm, while those with ZrO_2 passivation attain a higher maximum g_m of 160 mS/mm and a lower R_{on} of 10 Ω/mm. In addition, ZrO_2 passivation has helped to produce a higher I_{Dsat} despite a lower gate overdrive (2.7 versus 3 V), as depicted in Fig. 3(a). The shift in V_{th} seen in Fig. 3(b) is caused by the thermal treatment of the gate metal during the ZrO_2 deposited.

Conclusion

In conclusion, we have fabricated InAlN/GaN Schottky gate HEMTs grown on Si (111) substrate with non-gold based contacts (Ti/Al/Ni/W ohmic and Ni/W Schottky) and their performance seems comparable to devices with gold-based contacts. We have also demonstrated that a thin ZrO_2 passivation layer helps improve the DC characteristics of InAlN/GaN HEMT.

References

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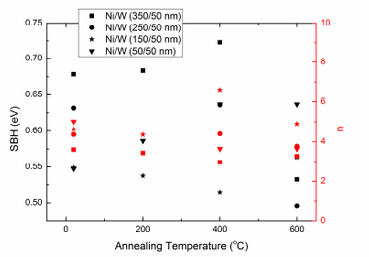

Fig. 1: Effect of Ni/W thickness ratio and annealing temperature on SBH.

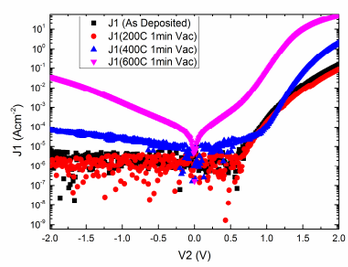

Fig. 2: Annealing temperature dependent I-V characteristics of Ni/W (350/50 nm) Schottky Diodes.

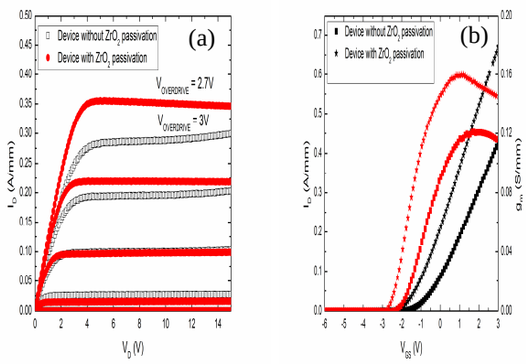

Fig. 3: (a) I_{DS}-V_{DS} and (b) I_{DS}-V_{GS} @ V_{DS} = 10V of InAlN/GaN HEMT with and without ZrO_2 passivation.