InGaSb MOSFET Channel on Metamorphic Buffer: Materials, Interfaces and Process Options

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Development of p-type MOSFETs using new materials is an important goal to provide further scaling of CMOS circuits. Although Ge is still considered as a main candidate for novel p-channels due to its superior bulk transport properties, recent progress in strained III-Antimonides channels and MOS technologies makes III-Sb materials a good competitor in particular for deeply scaled devices. The materials parameters affecting MOSFET's figures-of-merit are reviewed with the emphasis on strain in quantum wells (QWs), effective mass, density of states and mobility.

Progress in development of materials for III-Sb channels is reported. Optimization of MBE growth of metamorphic buffers and GaSb on lattice-mismatched GaAs substrates has resulted in "step-flow" growth mode of GaSb with monolayer-high steps on the surface, ~10^7cm^{-2} dislocation density and bulk hole mobility 860 cm^2/Vs [1]. Strain optimization in QWs provided the highest Hall mobility of 1020 cm^2/Vs at sheet hole density of 1.3x10^{12}/cm^2 obtained for $In_{0.36}Ga_{0.64}Sb$ with compressive strain of 1.8%. An important figure-of-merit of InGaSb QWs relevant to MOSFETs is the lowest sheet resistance, ~3.9 kΩ/sq. that was observed at hole density 1.9x10^{12} cm^{-2}.

Hole mobility in QW channel with Al_2O_3 high-k gate oxide (Fig.1) was benchmarked against the thickness of top semiconductor AlGaSb barrier (Fig. 2). The results in Fig.2 show just a minor 30% drop of the mobility from over 1000 cm^2/V-s in the structures with 50 nm thick top barrier layers to ~700 cm^2/V-s in the surface channel devices. This drop is significantly less than 5-7 times mobility degradation in surface n-type InGaAs channels reported recently. This result is quite encouraging and may serve as a feasibility proof that the "high hole mobility" properties will be preserved in inversion and fin-channel p-type MOSFETs.

Two approaches to fabricate high-quality III-Sb/high-k interface were studied: all in-situ Al_2O_3 or HfO_2 gate oxides, and ex-situ atomic layer deposited (ALD) Al_2O_3 with InAs top semiconductor capping layer. Interface with in-situ MBE gate oxides was found to improve with in-situ deposited a-Si interface passivation layer (IPL). Interfaces with better thermal stability, reduced interface trap density and hysteresis were observed on both n- and p-type GaSb MOSCaps with the IPL. P-type MOSFETs with HfO_2 showed a maximum drain current of 23 mA/mm for a 3μm gate length.

An interface with ALD Al_2O_3 was improved by a thin 2nm interface layer of InAs which was treated with HCl or $(NH_4)_2S$ immediately prior to ALD process [2]. Optimized annealing further improved the C-V characteristics, reduced interface trap density down to 10^{12} cm^{-2}eV^{-1} (Fig.3), leakage current and MOSFET subthreshold slope down to 180 mV/dec. Increasing annealing temperature above ~450°C drastically degraded C-V characteristics indicating low thermal budget of antimonides. This degradation corresponds to increased oxidation of the interface as observed by XPS (Fig.4).

[1] V. Tokranov, S. Madisetti, M.Yakimov, P.Nagaiah , N. Faleev, and S.Oktyabrsky, J. Cryst. Growth **365**, (2013).
[2] A. Greene, S. Madisetti, P. Nagaiah, M. Yakimov, V. Tokranov, R. Moore, and S. Oktyabrsky, Solid State Electron. **78**, 56 (2012).

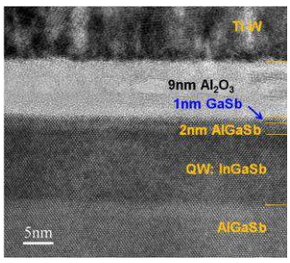

Fig.1. Cross-sectional TEM micrograph of the strained $In_{0.36}Ga_{0.64}Sb$ QW structure with 3nm thick top barrier (2nm AlGaSb+1nm GaSb) and 9 nm Al_2O_3 gate oxide.

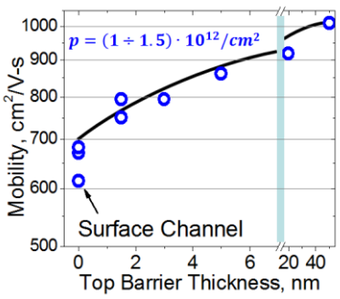

Fig. 2. Room temperature Hall mobilities in strained $In_{0.36}Ga_{0.64}Sb$ QWs with $Al_{0.8}Ga_{0.2}Sb$ barriers and Al_2O_3 gate oxide as a function of semiconductor top barrier layer thickness that included 1nm GaSb capping.

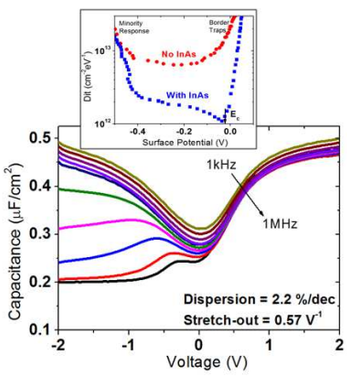

Fig. 3. Capacitance-voltage characteristics of GaSb/InAs/Al_2O_3 MOSCap. Inset: Dit extracted from high-low frequency method for n-GaSb MOSCaps with and without InAs (2nm thick) passivation.

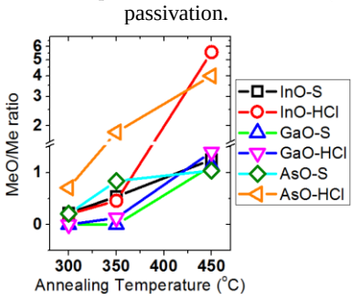

Fig. 4. Ratio of metal-oxide/metal XPS lines of Al_2O_3(1.5nm)/InAs/GaSb vs. annealing temperature showing thermal degradation of the gate stack and effectiveness of $(NH_4)_2S$ with respect to HCl treatment.