III-V/High-k Defects: DIGS vs. Border Traps <u>C. L. Hinkle¹</u>, R. V. Galatage¹, D. M. Zhernokletov¹, H. Dong¹, S. R. M. Anwar¹, B. Brennan¹, R. M. Wallace¹ and E. M. Vogel² ¹Department of Materials Science and Engineering University of Texas at Dallas Richardson, Texas, USA ²Georgia Institute of Technology

High mobility, III-V based, metal-oxidesemiconductor (MOS) transistors are being considered for next generation technologies. Recent advances in processing, such as atomic layer deposition of high-k dielectrics, has allowed for the fabrication of promising devices. Frequency dispersion in accumulation is a commonly observed feature in the experimental capacitance-voltage (C-V) characteristics of III-V MOS devices. This characteristic has been reported on a wide variety of III-V substrates in conjunction with many different dielectrics. The conventional interface state capacitance (Cit) model, which works extremely well for Si devices, does not accurately model the frequency dispersion observed in III-V systems. Different models have been developed to explain the origin of this frequency dispersion.

One model, disorder induced gap states (DIGS), attributes this dispersion to the tunneling of carriers into a disordered region caused by oxidation of the III-V substrate which is close to the interface between the III-V substrate and an insulator.^{1,2} A separate model attributes this dispersion to border traps located inside and associated with the high-k dielectric.^{3,4} In this work, we fabricated MOS devices utilizing both HfO2 and Al2O3 on In_{0.53}Ga_{0.47}As and InP substrates and correlate device characteristics with interface chemical bonding through in-situ x-ray photoelectron spectroscopy (XPS). Through this analysis, it is shown that the observed frequency dispersion must be due to the disruption of the crystalline III-V semiconductor during oxide deposition and not due to border traps located in the high-k dielectrics.

MOS capacitors were fabricated on n-In_{0.53}G_{0.47}As and n-InP substrates with HfO₂ and Al₂O₃ dielectrics. Room temperature ammonium sulfide was used for surface passivation prior to ALD. Room temperature C-V characteristics (Fig. 1) show a large interface trap response for InGaAs and InP devices with both HfO₂ and Al₂O₃ dielectrics. A semi quasi-static method, utilizing variable temperature and variable frequency measurements, is used to calculate the D_{it} distribution across the band gap of both substrates (Fig. 2). Details of the technique will be presented. For the InGaAs devices, the magnitude of the extracted midgap and conduction band (CB) D_{it} is higher for those devices with HfO₂ as the insulator as compared to those with Al₂O₃. XPS analysis of the InGaAs samples confirms the increased presence of Ga-oxidation states, As-As



Fig. 1 C-V measurements showing frequency dispersion.



Fig. 2 Extracted Dit for InGaAs and InP with HfO2 or Al2O3.

bonding, and Ga-dangling bonds in the case of the HfO₂ relative to the Al₂O₃ (Fig. 3). In contrast, for the InP devices, the magnitude of the extracted midgap and CB D_{it} is higher for the Al_2O_3 than the HfO₂, opposite of the InGaAs characteristics. XPS analysis of the InP samples illustrates that more interfacial phosphate bonds are formed with the Al_2O_3 relative to the HfO₂ (Fig. 4). The two dielectrics give different results for CB D_{it} on two different substrates. This suggests that border traps in the high-k oxide are not responsible for the observed frequency dispersion.



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 P_2p

InPO,

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Fig. 4 XPS spectra showing increased phosphates for Al₂O₃/InP.