# Effect of Different Patterns for Epitaxial Lift-Off Process by Finite Element Method

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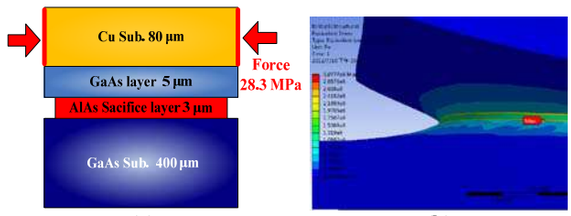
## Abstract

In this study, using the finite element method analyzes stress and strain of device structure on different patterns epitaxial lift-off process. Design copper substrate bears stress 28.3 MPa and to simulate the change of the sacrificial layer in the epitaxial lift-off process, which setting the sacrificial layer etching amount for 10%, 30%, 50%, 70%, 90%. Besides, the stress and strain distribution of device structure analyzes on various sacrificial layer etching amount. From the results found that the copper substrate suffered different stress distribution. Copper substrate and GaAs substrate are protected by a tensile stress. Copper substrate is subject to tensile stress and its corner exist the maximum of stress and strain. Moreover, the stress distribution of epilayer concentrates in the upper and lower interface of sacrificial layer. The stress is larger sacrificial layer etching to 10% than etching to 90%. From stress contrast of these four structures on epitaxial lift-off process, the structures 3 stress is relatively lower, which the stress reduces approximately half on etching amount 50%. Therefore, the GaAs epilayer not only reduce subjected to stress but also decrease the occurrence of defects.

## Introduction

In presently, the application of III-V solar cells, light-emitting diodes and laser diodes chip, which general using epitaxial lift-off process technology transfer epitaxial film to metal substrate for to enhance thermal conductivity of substrate. It causes breakage of the epilayer and deterioration of the quality due to the effects of different the residual stress and thermal expansion coefficient on GaAs with Copper substrate. Since previous research[1][2], from GaAs epilayer discover cracked phenomenon after epitaxial lift-off process. In order to improve this problem, and design different device structures simulate stress and strain distribution behavior by finite element method. By the design of device structure effectively reduces of the stress distribution in the GaAs epilayer. Fig. 1(a) simulate device structure diagram, which design the sacrificial layer amount 10%~90% for simulation the stress and strain distribution of the etching process. Fig. 1(b) show the stress distribution of cubic structure with maximum stress is on sacrificial layer. Fig. 2 Show the deformation morphology of various structures on sacrifice layer etching 50%, and center hole of structure 2 can to enhance etching rate. In Fig. 3, with the advance of sacrifice layer etching amount the stress gradually decrease. Moreover, the stress of structure 3 decreases about 50% than other structure on sacrifice layer etching 50%. Therefore, the structure 3 demonstrates to reduce stress by finite element method.




(a) (b)

Fig. 1 (a) Simulate device structure diagram, (b) the stress distribution of cubic structure.

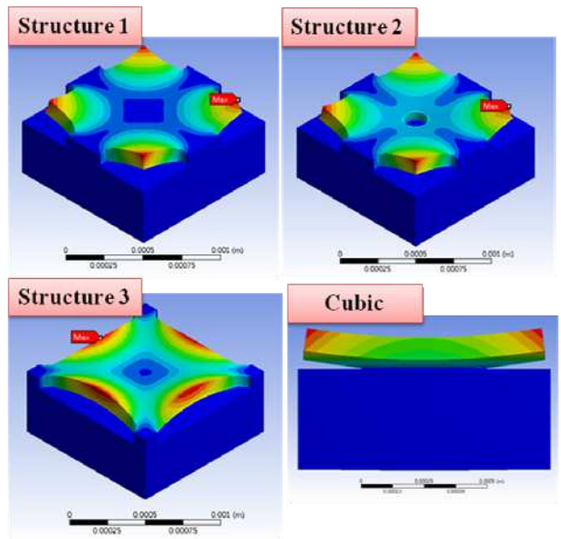



Fig. 2 Deformation morphology of various structures on sacrifice layer etching 50%.

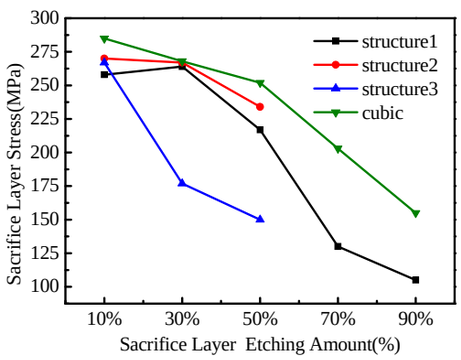



Fig. 3 Sacrifice layer stress of various structures depended sacrifice layer etching amount.

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## References

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