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Si-SiO_2 Interface to High-*k*-Ge/III-V Interface: Passivation and Reliability

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For MOS devices, the oxide-semiconductor interface needs to be defect free and should be highly reliable. Various process conditions significantly impact the nature of this interface. Device scaling requirements introduced plasma etching in silicon processing in 1980s when the device sizes were in 1 µm range. Plasma-processing induced damage became a serious reliability issue of Si-SiO_2 interface. The energetic ions and photons produced by the glow discharge plasma were forming trapping centers for electrons and holes at the Si–SiO_2 interface. Capacitance–voltage (C–V) measurement and deep level transient spectroscopy (DLTS) were able to detect the interface traps and the bulk defect centers adjacent to the Si–SiO_2 interface (Fig. 1). The other major source of plasma damage in MOS structures was the current stress to the oxide. This effect impacted the hot carrier lifetime degradation depending on polarity of current stress during plasma damage. Hydrogen was able to passivate most of the interface defects and dangling bonds at the Si–SiO_2 interface. Introduction of deuterium at the Si-SiO_2 interface by annealing or implantation also improved the hot carrier reliability [2]. Nitrogen incorporation at the Si-SiO_2 interface enhanced the interface quality and the gate oxide reliability further. Plasma damage became a non-issue when the thickness became very low and design requirements adapted to antenna rules. SiON became the main dielectric for high performance devices but power consumption became severe because of direct tunneling.

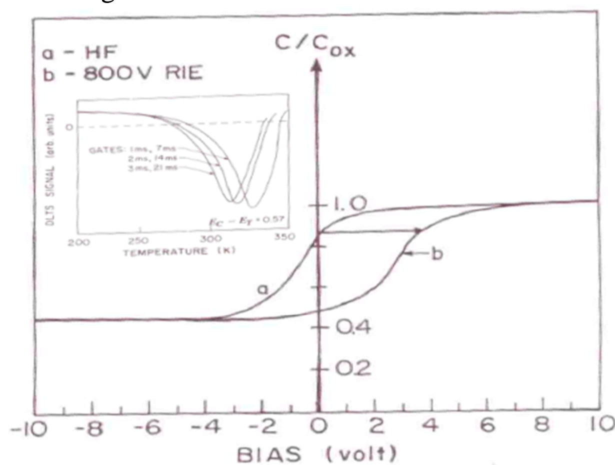

Fig. 1 Flat-band voltage shift and interface defect (inset) due to plasma processing damage.

For high speed and low power applications materials with high-k dielectric constant such as Hf-based dielectrics are being integrated into standard CMOS technologies. That introduced a difficult challenge to Si-high-k interface. Some type of SiO_2 maintained its presence at the interface (interfacial layer) keeping the properties of Si–SiO_2 interface. Negative bias temperature instability (NBTI) was an issue for pMOS devices but with high-k gate dielectrics positive bias temperature instability (PBTI) became a reliability concern

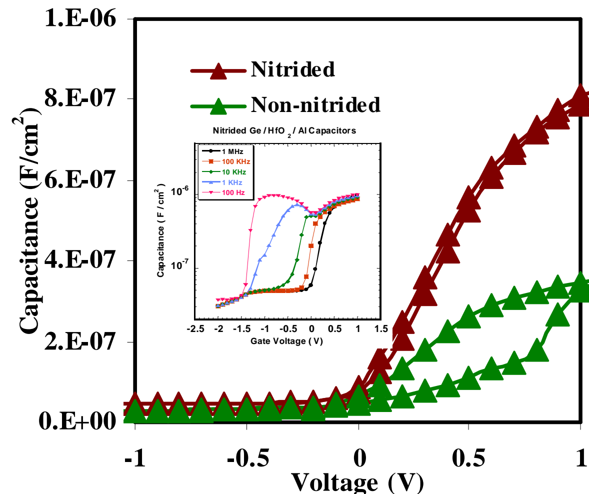

Fig. 2. Reduction of hysteresis but frequency dispersion (inset) of nitrogen treated high-k-Ge interface.

To attend the ITRS intended transistor drive current for sub-22 nm CMOS technology and beyond high mobility channel materials are in the process of being integrated. Substrates such as germanium (Ge) and gallium arsenide (GaAs) are being considered for their high electron mobility. The interface between the high-k dielectrics and the high mobility substrates are not well understood as the knowledge of Si–SiO_2 interface is not much useful anymore. Various interface passivation techniques were used starting with nitrogen to optimize the device performance. However, it was not quite successful because of material incompatibility. To improve the high-k/Ge interface when interface treatments such as surface nitridation [3] was used to passivate interface it was useful in one aspect whereas detrimental in another (Fig. 2). Electrical characteristics of high-k on III-V substrates are still limited as the quality of high-k-III/IV interface. At present, device performance of high-k on III/V has not exceeded the nanoscale Si devices with high-k gate stacks [4]. Enhancement of electrical performance in these devices, therefore, will be possible when the deposition process, precise selection of deposition parameters, predeposition surface treatments and subsequent annealing temperatures are simply optimized.

References

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