

Sharp-Switching High-Current Tunneling Devices

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Tunneling FETs offer the possibility overcoming the 60 mV/decade subthreshold slope (SS) limit of conventional transistors and thereby providing sharp-switching logic devices. They are also ideally suited to ultrathin channel SOI technology since interband tunneling depends near-exponentially on the maximum electric field E_{MAX} controlled by the gate voltage V_G . However, to date, experimentally demonstrated Si TFETs have exhibited an unacceptably low on current I_{ON} , due to the large tunneling barrier arising from the Si bandgap.

This presentation will discuss two approaches for increasing the TFET I_{ON} , both using bandgap engineering in the CMOS-compatible Si/Ge system.

In the bipolar-enhanced TFET (BET-FET),¹ the V_G -controlled tunneling current is amplified via the current gain in a Si/SiGe heterojunction. This leads to a compact device with high simulated $I_{ON} > 10^3 \mu\text{A}/\mu\text{m}$, SS < 60 mV/decade over many orders of output current, and a low I_{OFF} as in a floating-base transistor. A number of SOI-compatible device variants is possible, including both vertical and lateral current layouts, and simulations show the device to be scalable down to sub-20 nm dimensions. The BET-FET outperforms both conventional CMOS and Si TFETs, but has not yet been demonstrated experimentally.

In the heteronanowire Si/Ge tri-gate TFET,² the I_{ON} is determined by E_{MAX} in the lower bandgap Ge section, while the I_{OFF} is due to the weaker tunneling in the Si section. Preliminary top-gated high-k insulated prototypes, grown by vapor-liquid-solid epitaxy and fabricated via e-beam lithography on an oxide-covered Si substrate, show reasonably high $I_{ON} > 1 \mu\text{A}/\mu\text{m}$ and good SS. A fully CMOS-compatible process flow combining VLS epitaxy with vertical gate formation remains to be developed.

¹J. Wan *et al.*, "Novel bipolar enhanced TFET (BET-FET) with simulated high ON current", to appear in *IEEE EDL* (2012).

²Son T. Le *et al.*, " Axial SiGe heteronanowire TFETs", *Nano Lett.* **12**, 5850 (2012), doi: 10.1021/nl3032058.