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Challenges in 3D Integration

Mitsumasa Koyanagi[1], Kang Wook Lee[1], Takafumi Fukushima[1], and Tetsu Tanaka[2]
1New Industry Creation Hatchery Center,
Tohoku University
6-6-10 Aza Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
E-mail: koyanagi@bmi.niche.tohoku.ac.jp
Tel: +81-(0)22-795-6906
2Graduate School of Biomedical Engineering,
Tohoku University

Introduction

Three-dimensional (3D) LSIs using TSVs are indispensable to achieve high performance and low power LSIs with smaller form factor. A wafer-to-wafer (WtW) technology is suitable for stacking chips with high production yield such as DRAM since the overall yield after stacking rapidly decreases as the number of stacking layers increases. The chip-to-wafer (CtW) is suitable for stacking known good dies (KGDs). In addition, chips with different size which are fabricated using different process technologies can be stacked in the CtW technology. The inherent problem in the CtW technology, however, is low production throughput. To solve these problems, we have proposed a new 3D heterogeneous integration technology called a super-chip technology using self-assembly and electrostatic (SAE) bonding method [4].

Heterogeneous Integration and 3D Superchip

Super-chip technology makes possible to merge different kinds of technologies such as packaging, MEMS, photonics and so on as shown in Fig.1. A new self-assembly and electro-static (SAE) bonding method is employed in this super-chip technology for stacking various kinds of chips with different chip size and chip thickness which are fabricated using different process technologies. A number of chips are simultaneously aligned and bonded with high alignment accuracy of less than 0.5µm by making use of the surface tension of liquid and electrostatic force.

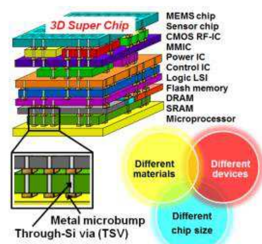


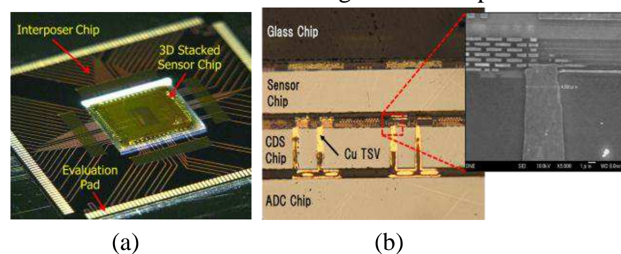
Fig.1 3D super-chip.

SAE (Self-Assembly and Electrostatic) Bonding

KGDs are directly carried from a tested wafer to an electrostatic multichip carrier (e-carrier), and then are released onto water droplets provided on hydrophilic bonding regions formed on the e-carrier. Thus many KGDs are precisely self-assembled on the e-carrier. After self-assembly, the KGDs are temporarily bonded to the e-carrier by electrical charging with high DC voltage. Then, the e-carrier with the KGDs is aligned and temporarily bonded to the corresponding support wafer on which a temporary adhesive is coated. In a multichip-to-wafer (MCtW) technology using Self-Assembly and Electro-static (SAE) bonding, the temporarily bonded many KGDs are readily debonded from the e-carrier and transferred to the support wafer by discharging the voltage. The subsequent processes are resin molding, multichip thinning, TSV/microbump formation, and second multichip transfer from the support wafer to the corresponding target LSI wafer. The temporary adhesive used in this process has high thermal stability whereas glued chips can be easily removed from the support wafer after TSV formation. By repeating the sequence, we can obtain 3D stacked thin chips with TSVs.

Fabrication of Heterogeneous 3D LSI

We have been developing various kinds of hetero-geneous 3D LSIs using 3D super-chip technology. A 3D-stacked image sensor chip is one example of these heterogeneous 3D LSIs. Our 3D-stacked image sensor chip is composed of CMOS image sensor (CIS) layer, correlated double sampling circuit (CDS) layer, and analog-to-digital converter (ADC) array layer. One image frame with 320×240 pixels is divided into 20×15 image processing blocks. Each block is composed of 256 CIS pixel circuits, one CDS circuit, and one ADC circuit which are electrically connected TSVs. The CIS chip was fabricated using 0.18-µm front-side illumination CMOS image sensor technology. Each pixel is designed with 10µm×10µm size and one image processing block has 255 pixels and one Cu TSV with the diameter of 5µm. The CDS chip and ADC chip were fabricated using 0.18-µm CMOS technology and 90-nm CMOS technology, respectively. Each chip has $5{\times}5mm^2$ size. We stacked these chips by a novel chip-based heterogeneous integration technology. The comer-cially available 2D chips are processed and integrated in chip-level. First of all, before stacking three kinds of chips, Cu/Sn microbumps are formed on the surface of each chip. Each functional chip with Cu/Sn microbumps is glue-bonded temporally to a supporting glass substrate and thinned down to 40µm thickness. Via holes with 5µm dia. are etched from the backside of Si substrate. The dielectric liner at the bottom of hole is etched by dry etching. Then holes are filled with Cu by elctroplating. Next Cu and Sn electroplating are used to form backside Cu/Sn microbumps. By repeating these processes, we fabricated 3D-stacked image sensor. The bird's-eye view and cross-sectional image of the fabricated 3D-stacked image sensor are shown in Figs. 2 and 3. We have confirmed basic function of this 3D-stacked image sensor chip.



(a) (b)

Fig.2 3D-stacked image sensor chip

Conclusion

We have proposed a new 3D heterogeneous integration technology called a super-chip technology using SAE (Self-Assembly and Electrostatic) bonding which makes use of the surface tension of liquid for chip alignment and the electrostatic force for bonding. We have fabricated and evaluated a 3D-stacked image sensor chip as one example of heterogeneous 3D LSIs using 3D super-chip technology.

Acknowledgement

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References

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