Metal Gate/High-k Dielectric Gate Stack Reliability; Or How I Learned to Live with Trappy Oxides.

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INTRODUCTION

Over the last couple of scaling generations the gate stack in leading edge technology has migrated from Poly-Si and SiON to a metal gate with a bi-layer of a Hafnium based dielectric with a SiON interlayer (IL). This switch yielded immediate gains in gate leakage (I_g) and reliability, allowing a thinning of the inversion thickness (t_{inv}) from ~20Å to less than 14Å. Even though gate length scaling and performance would drive further thinning of the dielectric stack, reliability considerations limit this. Understanding the fundamental reliability mechanisms enables mitigation with process changes and an optimization of reliability, performance, and operating voltage (V_{max}). This paper will explore the main reliability mechanisms that are limiting scaling and the processes that improve reliability. Furthermore, the relationship between device level reliability and circuit reliability will be broached with ring oscillator data that shines light on the dominant reliability mechanism limiting V_{max}.

RELIABILITY MECHANISMS

The main reliability mechanisms that limit t_{inv} scaling are bias temperature instability (BTI) for both NFETs (PBTI) and PFETs (NBTI), and NFET dielectric breakdown (nTDDB). PBTI is directly caused by bulk electron trapping at oxygen vacancies in the thick hafnium based dielectric top layer, while NBTI is the result of hole trapping in the SION IL and interface trap generation at the silicon interface. nTDDB is directly controlled by the dielectric layer thicknesses and the resulting gate leakage current density. Intensive research by a multitude of groups has uncovered multiple ways to reduce these mechanisms. Reducing the high-k thickness or mixing the high-k with rare earth metals reduces PBTI (Fig. 1) [1]. Decreasing the nitrogen in the IL or using a SiGe channel for the PFET reduces NBTI (Fig 2) [2]. nTDDB is primarily driven by I_g, so process changes that reduce Ig will increase TDDB reliability. Furthermore, all of these mechanisms are driven by the electric field (E_{ox}) in the gate oxide. Altering the workfunction of the metal gate towards the silicon mid-gap reduces E_{ox} yielding gains for all three reliability mechanisms. Combining the voltage scaling of each mechanism, V_{max} trends can be predicted for future technologies.

It will also be shown that while Gate-First and Gate-Last high-k/Metal gate stacks have differing thermal budgets and workfunction metals, reliable gate stacks can be obtained in either integration scheme [3, 4].

VMAX and RING OSCILLATORS

The two largest challenges with gate dielectric reliability are projecting reliability to end of life and extending device level models to predict circuit reliability. To this end, we have developed specialized Ring Oscillator (RO) structures that isolate the effects of NBTI and PBTI on frequency degradation (Fig. 3) [5], closing the gap between device and circuit level models.

CONCLUSION

Understanding the reliability mechanisms of Metal Gate/High-k dielectric gate stacks enables mitigation and an optimization of reliability with performance in future scaling generations.

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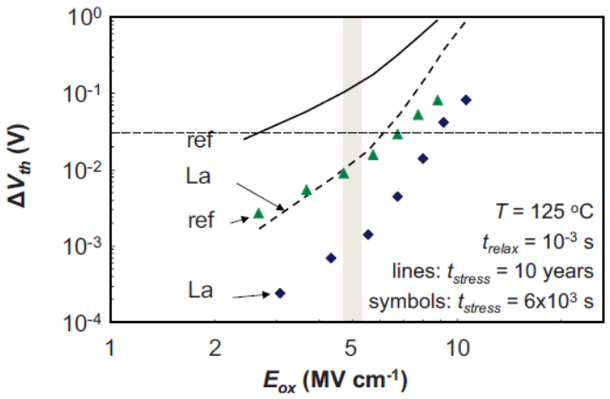

Fig. 1 Adding Lanthanum to Hf based dielectrics significantly reduces PBTI, improving the projection by > 5x. from [1]

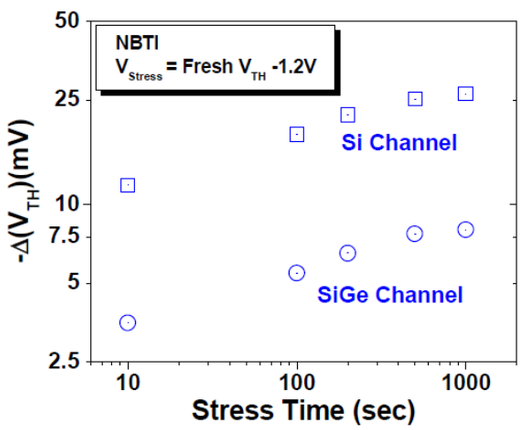

Fig. 2 NBTI can be improved significantly with a SiGe channel as compared to a traditional Silicon channel. from [2]

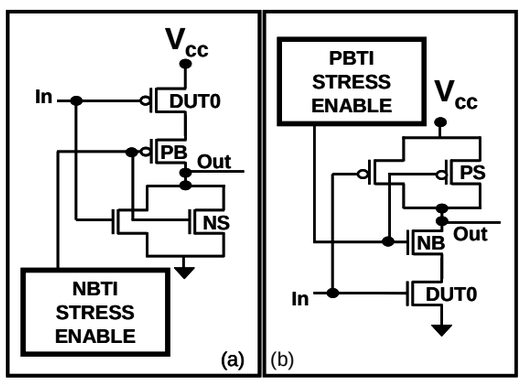

Fig. 3 Specialized RO structures. (a) NOR style circuit that stresses only the PFET DUT. (b) NAND style circuit that stresses only the NFET DUT. from [5]