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FinFET Patterning Process Challenges

Efraín Altamirano-Sánchez and Nadine Collaert

IMEC
Kapeldreef 75 B-3001 Leuven Belgium

Since the finFET architecture is after all a strategy to overcome the scaling issues [1], semiconductor industry has explored two fin flavors: starting from a silicon on insulator substrate (SOI finFET) or from a bulk substrate (bulk finFET). Bulk finFET uses a fabrication scheme very close to standard bulk processing: after the shallow-trench-isolator (STI) etching, the STI oxide is recessed in order to define de fin height. For both fins, the etching processes are very similar, except for the final etching step, where the etch stops on SiO_2 for SOI fin or stops in the Si substrate in the case of bulk finFET .

The scaling down of the fin layout dimensions has been possible thanks to different lithographic approaches. For example the patterning techniques that we have used for reducing the fin pitch from 350 nm to 30 nm are: 193 ArF lithography, 193 immersion (193i) lithography and EUV lithography (EUVL). For the smallest dimensions 193i or EUV lithography has been combined with spacer defined double patterning (SDDP). Table 1 shows the fin dimension, logic node technology and pitch that we have explored. During this exploration, we have learned that the plasma etching processes become more and more complex and right now ICP type etching reactors are reaching their limits. New gadgets such as pulse plasma, pulse bias, multi-zone electrostatic chuck temperature, lateral gas injection, etc. might be needed for fulfilling semiconductor industry needs.

So it is clear that the finFET architecture leads to a more complex plasma etching processing, especially for small pitches (<64nm) and fins with critical dimensions (CD) below 15 nm. Straight profiles are needed for controlling the short channel effects (SCE) [2], this makes the fin patterning more challenging when the structure density increases (i.e. 45nm pitch) and the CD is scaled down to 10 nm. One of the most critical dry-etching challenges for reaching sub-15 nm wide fins is to transfer the photoresist (PR) mask pattern into to the hard mask (HM) and reduce the line width to the target dimension. For doing this, the PR pattern is transferred into the HM and then the HM is trimmed down to the fin CD target. Once the HM has the correct CD, its pattern is transferred into the silicon. The etching process has to cope with the photoresist line-edge-roughness (LWR) created after the lithography exposure. As the dimension is scaled down, the LWR becomes more relevant than never before. For improving the LWR, some plasma treatments have been developed, such as HBr, Ar and H_2. In figure 1, the effect of the H_2 plasma treatment on EUV PR is shown. The fin CD variation in Fig.1 (a) is a clear indication of high LWR while the fin CD variation in Fig.1 (b) is negligible due to a proper PR plasma treatment. As the fin dimensions are scaled down, this problem will be of extreme importance, where fast, economically viable and effective solutions are needed.

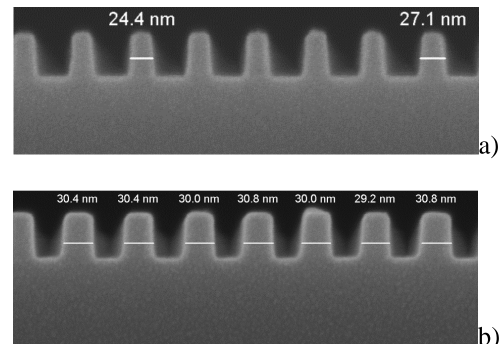

Fig.1 a) XSEM image of a silicon fins in a 30nm half pitch (SOI finFET) without (a) and with (b) PR plasma treatment

In this paper, we present the evolution of the plasma etching processes and the problems encountered for patterning fins for nodes between 130 nm node and 14 nm. In other words, from a “relax” fin pitch of 350 nm to an aggressive 45 nm pitch. We will also present the fin patterning challenges and the possible solutions to achievea fin pitch of 30nm.

References

[1] CMOS Nanoelectronics: Innovative Devices, Architectures and Applications. Nadine Collaert, Pan Standford Publishing, 2013.
[2] M.J.H. van Dal, et al. ESC Transactions, 13 (2008) 223.

Lithography	Logic Technology node	Fin pitch (nm)	Lithography Fin CD (nm)	Etching fin CD (nm)
193 SOI fin	130	350	78	35
	65	200	78	25
193i SOI fin	32	125	45	23
	22	90	40	17
EUV SOI fin	s22	80	40	15
	16	64	35	13
193i+SDDP Bulk Fin	14	45	45	10
EUV+SDDP Bulk Fin	10	30	30	7

Table 1. Fin dimension and the patterning strategy for SOI or bulk finFET.