III-V compound semiconductors for Scaling of Logic Transistors

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In order to continue and maintain the pace of energy efficient transistor scaling, it is imperative to scale the supply voltage of operation concurrently. However, the supply voltage scaling has slowed in recent years due to two fundamental reasons: 1) lower operating electric field results in lower carrier velocity and, hence, less transistor drive current, and 2) lower threshold voltage results in exponentially rising leakage power. Fig. 1 plots the published intrinsic n and p-channel transistor performance (as measured from the unity gain cutoff frequency, f_T) from leading edge CMOS process technologies and their physical gate length spanning across the last two decades. It is evident that, over the last two technology generations, the rate of transistor intrinsic performance improvement has slowed as well as the gate length scaling rate capability. Such a trend is alarming since it ultimately may halt the progress in logic integrated circuits. In this invited paper, we discuss two promising III-V device architecture, III-V Quantum Well MOSFET [1] and III-V Tunnel FET [2] that may provide high performance, low leakage and low operating voltage for sub 10nm transistor technology.

References:

1. A. Ali et al, presented at VLSI Technology Symposium, Honolulu, Hawaii, June 2012.
2. D. Mohata et al, presented at VLSI Technology Symposium, Honolulu, Hawaii, June 2012