Optimization of Cu damascene electrodeposition process in ULSI for yield and reliability improvement

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## Abstract

Cu damascene electrodeposition is widely used in the microelectronics industry. A void-free fill electrodeposition process becomes increasingly crucial with the miniaturization of feature dimensions. We report here that by using a partial fill partitioning method, we can detect time-zero plating defects more effectively than PLY or cross-section SEM after the completion of Cu plating or after CMP. It plays a critical role in optimizing the process for different technologies and different levels.

In Cu damascene electrodeposition process, electrodeposited Cu fills the sub-micron features in the super conformal filling mode described by T. Moffat et *al*.<sup>[1]</sup> This superfilling capability by electrodeposition enabled the interconnect integration with Cu metallization. <sup>[2, 3]</sup>The void-free fill of the feature is crucial for good reliability and BEOL (back-end-of-line) yield. Partial plating has been widely used by tool and chemistry manufacturers to evaluate superfilling capability by looking at the ratio of sidewall deposition versus the bottom up deposition thickness. We will report here that partial fill partitioning of the process can also provide key information of time-zero plating defects, which seem to disappear if the wafers are electrodeposited with the regular thickness in CMOS. We suspect that the disappearing of the voids is due to the room temperature recrystallization of Cu with the full overburden. We speculate the time-zero voids create a weak interface between Cu and liner which leads to massive yield degradation as well as reliability failure. By using partial fill method, we optimize our processes to be void-free at time zero (time-zero means when features are completely filled but without the thick overburden). Significant reliability improvement with the new processes are demonstrated, as well as lower defect in PLY and lower yield degradation.

## Reference:

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