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A Two-Step Electrical Degradation Behavior in α-InGaZnO Thin-Film Transistor

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Recently, amorphous indium-gallium-zinc-oxide (α-IGZO) TFTs have been widely investigated due to their high field mobility, wide band gap, good uniformity and room process temperature [1-2]. However, the main problem of α-IGZO TFT is its reliability. The reliability issues of α-IGZO devices have been investigated such as bias stress, illumination, defects, and environments [3-5]. The intrinsic factor of α-IGZO film caused the electrical instability of TFT device. The bias stress-induced electrical instability of α-IGZO TFT is the one of important issues. The electron trapping is usually explained for threshold voltage (V_{th}) instability under bias stress. Moreover, many research groups have been reported that V_{th} instability of α-IGZO TFT is attributed to gas molecules [6-7]. In this study, we demonstrated the effect of bias stress and environment on the V_{th} instability in the α-IGZO TFT device. A tow-step electrical degradation behavior in α-IGZO TFT devices was found under gate bias stress.

Figs. 1(a) and (b) show the transfer characteristics of α-IGZO TFT devices under -35 V and 35 V gate-bias stresses, respectively. The tow-step electrical degradation behavior in α-IGZO TFT devices was found under negative and positive stressing conditions during 2000 s, as shown in Figs. 1(c) and (d). After 100 s stress, the positive parallel V_{th} shifts of 0.16 V, 0.29 V and 0.37 V were observed under V_{GS}=-15 V, V_{GS}=-25 V and V_{GS}=-35 V stresses, whereas the V_{th} shifts of 0.29 V, 0.43 V and 0.59 V were found under V_{GS}=15 V, V_{GS}=25 V and V_{GS}=35 V conditions, respectively. Moreover, there are no significant changes in the electron mobility and subthreshold swing (SS). For longer stress time (2000 s), larger negative V_{th} shifts of 2.05 V, 3.70 V and 5.17 V were found in the stressing conditions of V_{GS}=15 V, V_{GS}= 25 V and V_{GS}=35 V, while smaller negative V_{th} shifts of 0.64 V, 1.35V and 2.32 V were observed in V_{GS}=-15 V, V_{GS}= -25 V and V_{GS}=-35 V conditions, respectively. The V_{th} shift of positive gate-bias stress is more significant than that of negative gate bias stress, which means that more electrons are injected into the gate oxide from the channel film during positive gate-bias stress compared to the electron injection from gate during negative gate-bias stress. We consider that the two-step degradation behavior of the threshold voltage is due to two different mechanisms. The positive V_{th} shift is due to the electron trapping at the interface between the dielectric film and the channel layer. The negative V_{th} shift can be attributed to the free electrons produced in the IGZO film during longer stress time.

Fig. 2(a) depicts the SIMS profiles of α-IGZO TFT. The measurement result directly demonstrated that a large number of hydrogen atoms were piled-up in the BCPL. These piled-up hydrogen atoms may be due to the diffusion of H_2O molecules in the back channel protective layer (BCPL). The schematic diagram of H_2O molecules induced extra electron carriers model for α-IGZO TFT device is illustrated in Fig. 2(b). After short stress time, charge trapping in the gate dielectric and/or at the channel/dielectric interface resulted in the positive shift in V_{th}. Based on the SIMS result, we supposed the H_2O molecules through AlO_x (passivation layer) and piled-up in the SiO_x layer (BCPL). During longer stress time, the negative shift in V_{th} may be due to the high-electric field-induced extra electron carriers from H_2O molecules. The extra electron carriers resulted in a high electron concentration in the back channel, thus causing a lower V_{th}. The procedure can be described by $H_2O \rightarrow 2H^+ + O^- + e^-$. The measurement results indicated that the AlO_x cannot resist moisture very well. The quality of passivation layer plays an important role on the electrical degradation behavior in α-IGZO TFT devices.

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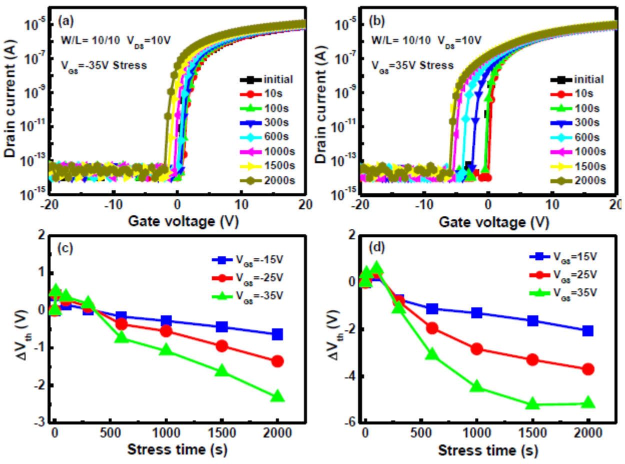

Fig. 1. Transfer characteristics of α-IGZO TFT devices as a function of stress times under (a) V_{GS}=-35 V and (b) V_{GS}=35 V stress conditions. Variations of the threshold voltage as a function of stress time for α-IGZO TFT devices under (c) negative and (d) positive gate-bias stresses.

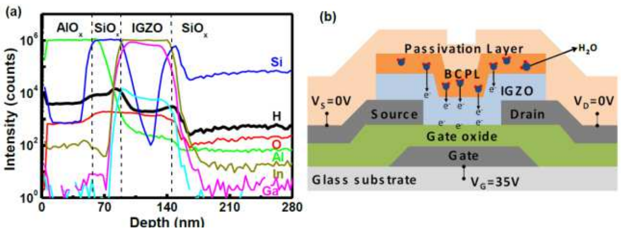

Fig. 2. SIMS profiles of the α-IGZO TFT device, (b) Schematic diagram of H2O molecules induced extra electron carriers model for an α-IGZO TFT device.