CdSe embedded ZrHfO gate dielectric nonvolatile memories – charge trapping and breakdown studies

Chi-Chou Lin and Yue Kuo
Thin Film Nano & Microelectronics Research Lab, Texas A&M University, College Station, TX 77843-3122

It was reported that the nanocrystalline Si (nc-Si) embedded high-*k* stack could replace the conventional poly-Si floating-gate dielectric stack in the nonvolatile memory (NVM) device to lower the operating power and to improve the reliability [1]. Many of the high-*k* film's inferior properties, such as the low crystallization temperature and the thick and defective interfaces, could be improved by the doping method, i.e., addition of a third element [2]. For example, when the Zr-doped HfO_2 (ZrHfO) was used as the gate dielectric layer in the MOS capacitor, its equivalent oxide thickness (EOT), effective *k* value, charge trapping, and interface density of states, etc. were better than those of the HfO_2 [2]. Among many available materials, CdSe is a possible charge trapping medium because it is a *n*-type semiconductor with a large work function, i.e., 4.8 eV to 5 eV [3]. In this paper, the charge trapping sites and reliability of the memory functions of the nc-CdSe embedded ZrHfO MOS capacitor were studied using the frequency dispersion method and the breakdown test.

The ZrHfO (tunnel oxide)/CdSe/ ZrHfO (control oxide) trilayer structure was sequentially sputter deposited on the *p*-type Si (100) wafer in a one pumpdown process. The ZrHfO and CdSe deposition conditions were as same as that in Ref. 4. The control sample, i.e., only the ZrHfO film without the embedded CdSe layer, was prepared for comparison. All samples were treated with a post deposition annealing (PDA) step at 800°C for 3 min under N_2 atmosphere. The ITO gate electrode was prepared by sputtering and wet etched into the 100 μm diameter pattern. The backside of the wafer was deposited with aluminum to form the ohmic contact. The post metal annealing was done at 400°C for 5 min under the H_2/N_2 (1/9) atmosphere.

The CdSe embedded ZrHfO MOS capacitor has been proved effective in trapping electrons with the positive gate voltage ($+V_g$) and holes with the negative gate voltage ($-V_g$). The charge trapping capability was large and the retention time was long [4]. In order to locate the charge trapping sites, the capacitor's *C-V* curves were measured from -6 V to + 6 V at 100 kHz, 500 kHz, and 1 MHz, separately, at room temperature. When the frequency was decreased, the *C-V* curve was stretched and shifted to the positive V_g direction, i.e., the flatband voltage V_{FB} moved from -0.29 V to 0.04 V. However, for the control sample, the *C-V* curve did not disperse with the frequency. This means that the bulk ZrHfO and Si/ZrHfO interface did not respond with the frequency at room temperature. The *C-V* stretch in the CdSe embedded sample was due to the slow response of the charges trapped in the shallow sites located at the CdSe/ZrHfO interface [2].

Figure 1 shows the *G-V* curves as a function of the measuring frequency for the nc-CdSe embedded ZrHfO MOS capacitor. At the flatband condition, both the density of the majority carriers and their capture rate are low, which causes the energy loss. Therefore, a conductance peak around V_{FB} is observed. The peak in Fig. 1 shifts to the $+V_g$ direction with the decrease of the measuring frequency, i.e., from -0.25V at 1 MHz to 0.15V at 100 kHz. This indicates that some charges may be trapped in the shallow sites at the nc-CdSe/ZrHfO interfaces and are physically close to the ZrHfO/Si interface. They respond to the low measurement frequency slowly and are easy to tunnel back to the Si substrate [2]. This phenomenon is consistent with the results in *C-V* measurements under different frequencies. For the control sample, the change of the peak location is negligible compared to that in the nc-CdSe embedded sample as shown in Figure 2. This is contributed by the relatively small amount of the interface states in the bulk ZrHfO film and the interface between ZrHfO film and the Si substrate [2].

The breakdown mechanism of the CdSe embedded memory device was investigated by the ramp-relax measurement [5]. At the beginning, a negative ramping voltage (V_{ramp}) was applied to the gate electrode, and a corresponding leakage current (J_{ramp}) was measured. After recording the J_{ramp}, the V_{ramp} was removed and a relax current (J_{relax}) was immediately measured. This procedure was repeated until the V_{ramp} reaches -10 V. The higher breakdown voltage was observed in the nc-CdSe embedded sample compared to that in the control sample i.e., -7.05 V for the former and -6.8 V for the later. This can be contributed by the larger film thickness of the former due to the extra 3 min CdSe deposition time. After the film was totally broken, the J_{relax} for the control sample jumped abruptly and changed the polarity since no charges were retained and the film became conductive. Oppositely, the J_{relax} for the CdSe embedded sample decreased slightly and the polarity remained the same after the breakdown. This phenomenon can be contributed to that some trapped charges still remained at the CdSe site even the bulk ZrHfO film was broken.

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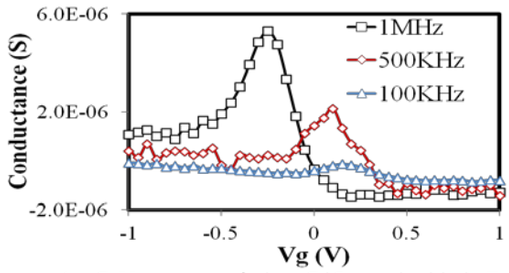

Figure 1. *G-V* curves of the CdSe embedded ZrHfO sample measure at 100 kHz, 500 kHz, and 1 MHz, 25°C

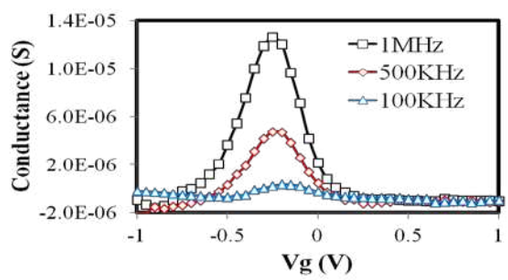

Figure 2. *G-V* curves of the control sample measure at 100 kHz, 500 kHz, and 1 MHz, 25°C